

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
6	0002265654	ENGINEERING RELEASED	2013-08-22

## SCHEM,MLB\_KEPLER,J45G

8/22/2013 DVT


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70	KEPLER FRAME BUFFER I/F	D2_MLB	07/31/2012
71	1V05 GPU / 1V35 FB POWER SUPPLY	D2_MLB	07/31/2012
72	GDDR5 Frame Buffer A	D2_MLB	07/31/2012
73	GDDR5 Frame Buffer B	D2_MLB	07/31/2012
74	KEPLER EDP/DP/GPIO	D2_MLB	07/31/2012
75	KEPLER GPIOs,CLK & STRAPS	D2_MLB	07/31/2012
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0675	1	SCHEM,MLB_KEPLER,J45G	SCH	CRITICAL	
820-3787	1	PCBP,MLB_KEPLER,J45G	PCB	CRITICAL	

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ABBREV=ABBREV  
LAST\_MODIFIED=Thu Aug 22 12:19:14 2013

DRAWING TITLE	
SCHEM, MLB, KEPLER, J45G	
 Apple Inc.	DRAWING NUMBER
	051-0675
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## BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0177	COMMON PARTS,MLB,KEPLER,J45	J45G_COMMON
985-0181	DEV,MLB,KEPLER,J45	J45G_DEVEL:DVT
639-5245	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5246	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5247	PCBA,MLB,KEPLER,CRW_BSET,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5248	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5249	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5250	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5251	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5252	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5253	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5254	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5255	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5256	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
639-5257	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5258	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5259	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5260	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5261	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5262	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5263	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5264	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5265	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5266	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5267	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5268	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
639-5478	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5479	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5480	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5481	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5482	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5483	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX
639-5484	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5485	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5486	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5487	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5488	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5489	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX

## J45G BOM Groups

BOM GROUP	BOM OPTIONS
J45G_COMMON	ALTERNATE,COMMON,J45G_COMMON1,J45G_COMMON2,J45G_PROGPARTS,GFX_BM,ACAPS:A2
J45G_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X8X8,S2_PWR:S0
J45G_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45G_PVT	BKLT:PROD,SENSOR_NONPROD:N
J45G_PROGPARTS	SMC_PROG:PROTO4,BOOTROM_PROG:PROTO4,TBTROM:PROG,TPAD_PSOC:PROG,GFX_PROGPARTS
GFX_PROGPARTS	DPMUXMCU:PROG
J45G_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,BKLT:ENG,DBGLED,CAM_XTAL:YES,DPMUX_DEBUG
J45G_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
GFX_BM	GK107:GX,DPMUX:HOCO
XDP_DEBUG	XDP_CONN,XDP_PCH

## Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	IC,CPU,CRW,PRQ,CO,2.0.47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	IC,CPU,CRW,PRQ,CO,2.3.47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	IC,CPU,CRW,PRQ,CO,2.6.47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,PCN,LPT-M, NM87,C2,8R199,PRQ,20x20mm,FCBG4	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR13C, FCBG4288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMBA,8XS,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	4Gb_HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4Gb_SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	4Gb_ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,Y80A,78P,FBGA		CRITICAL	4Gb_MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	4Gb_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4Gb_SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	4Gb_ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,Y80A,78P,FBGA		CRITICAL	4Gb_MICRON_1600
337S4256	1	IC,GPU,GK107-GT A2,BGA908	U8400	CRITICAL	GK107:GT
337S4427	1	IC,GPU,U107GX,926MHZ,1.0375V,1.5V,FBGA908	U8400	CRITICAL	GK107:GX
337S4616	1	IC,GPU,CK107-762,A2,940MHz,5GBps,1.2V,1.5V908BG	U8400	CRITICAL	GK107:GX2
333S0630	4	IC,SDRAM,DDR5,64MX32,A-DIE,HYNIX	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,DDR5,64MX32,D-DIE,SAMSUNG	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_SAMSUNG
333S0695	4	IC,SDRAM,DDR5,2GBIT,50MBps,1.70FBGA	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA
333S0701	4	IC,SDRAM,DDR5,2GBIT,50MBps,1.70FBGA,SDW2032BB8G-6A	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA_29nm
333S0734	4	IC,SDRAM,DDR5,64MX3,HYNIX,H50C2H248FP-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_29nm
333S0685	4	IC,SDRAM,DDR5,64MX3,HYNIX,H50C4H248FP-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX

DRAM SPD Straps

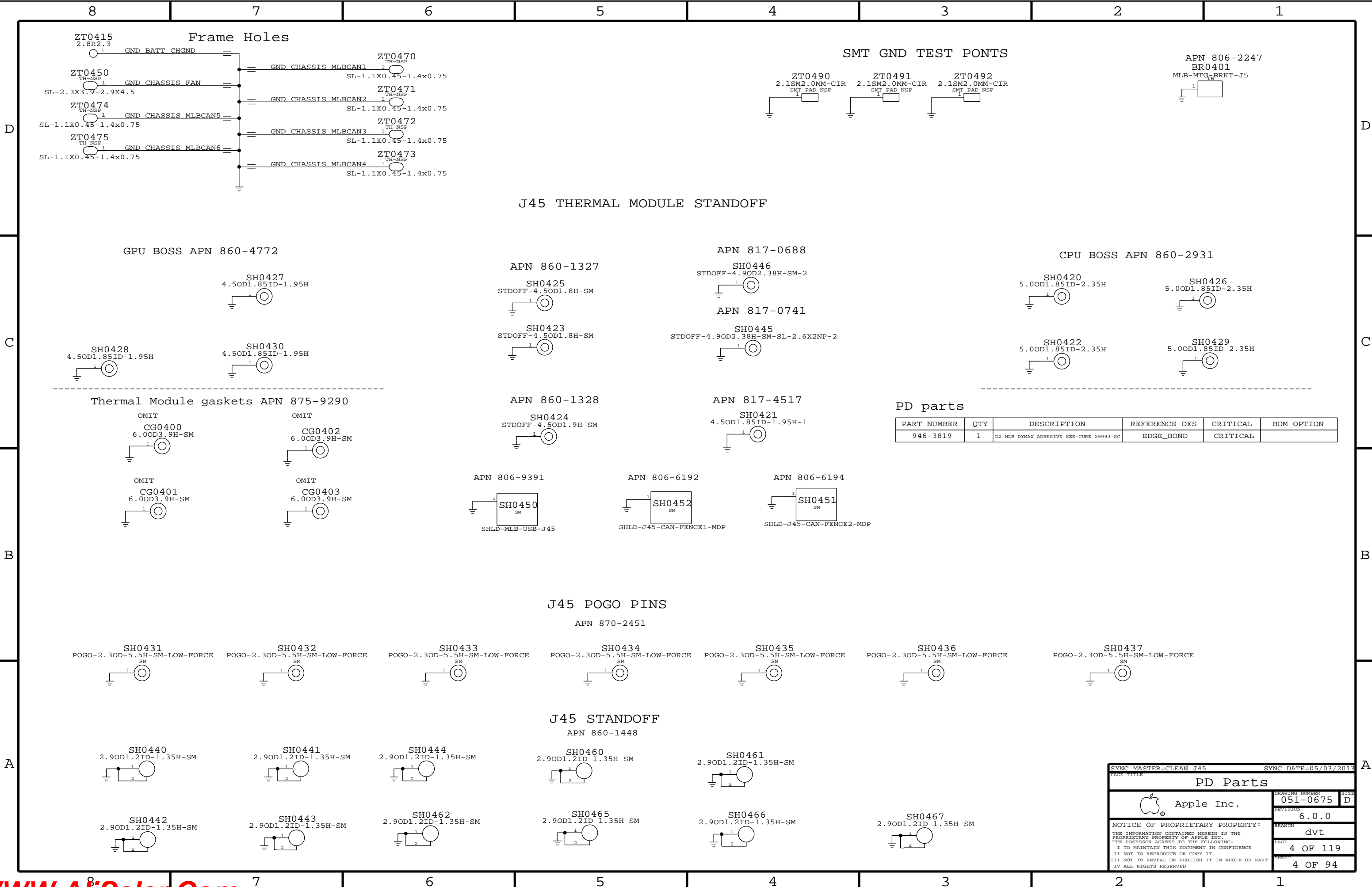
BOM GROUP	BOM OPTIONS
RAM:2Gb_HYNIX_1600	RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM:2Gb_SAMSUNG_1600	RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM:2Gb_ELPIDA_1600	RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM:2Gb_MICRON_1600	RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H
RAM:4Gb_HYNIX_1600_S	4Gb_HYNIX_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:L
RAM:4Gb_SAMSUNG_1600_S	4Gb_SAMSUNG_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:H
RAM:4Gb_ELPIDA_1600_S	4Gb_ELPIDA_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:L
RAM:4Gb_MICRON_1600_S	4Gb_MICRON_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H
RAM:4Gb_HYNIX_1600	4Gb_HYNIX_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM:4Gb_SAMSUNG_1600	4Gb_SAMSUNG_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM:4Gb_ELPIDA_1600	4Gb_ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM:4Gb_MICRON_1600	4Gb_MICRON_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H

## Development/Base BOM

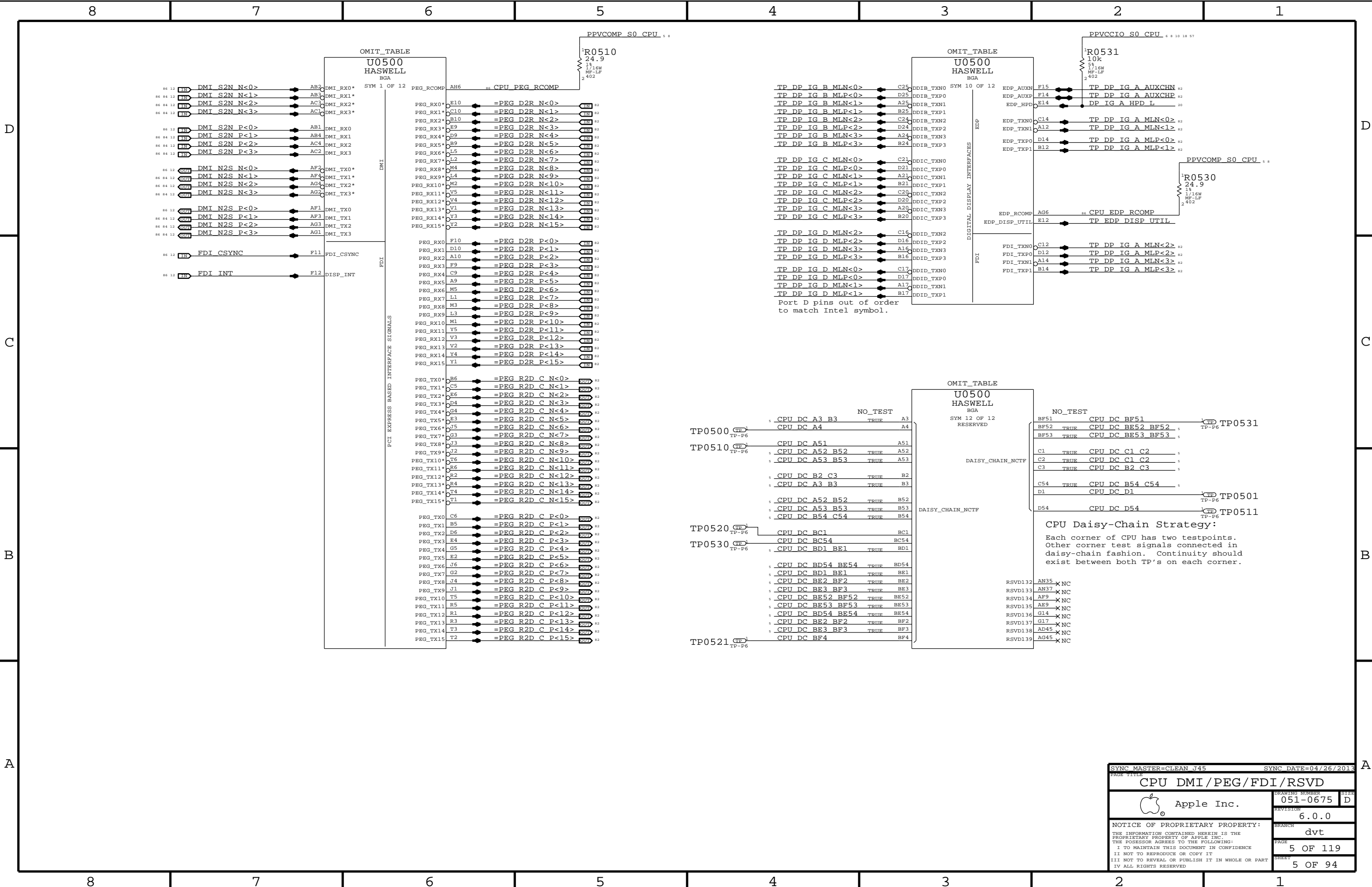
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0177	1	J45G MLB,KEPLER BASE BOM	BASE	CRITICAL	BASE_BOM
985-0181	1	J45G MLB,KEPLER, DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=J15 REFERENCE		SYNC DATE=07/31/2012	
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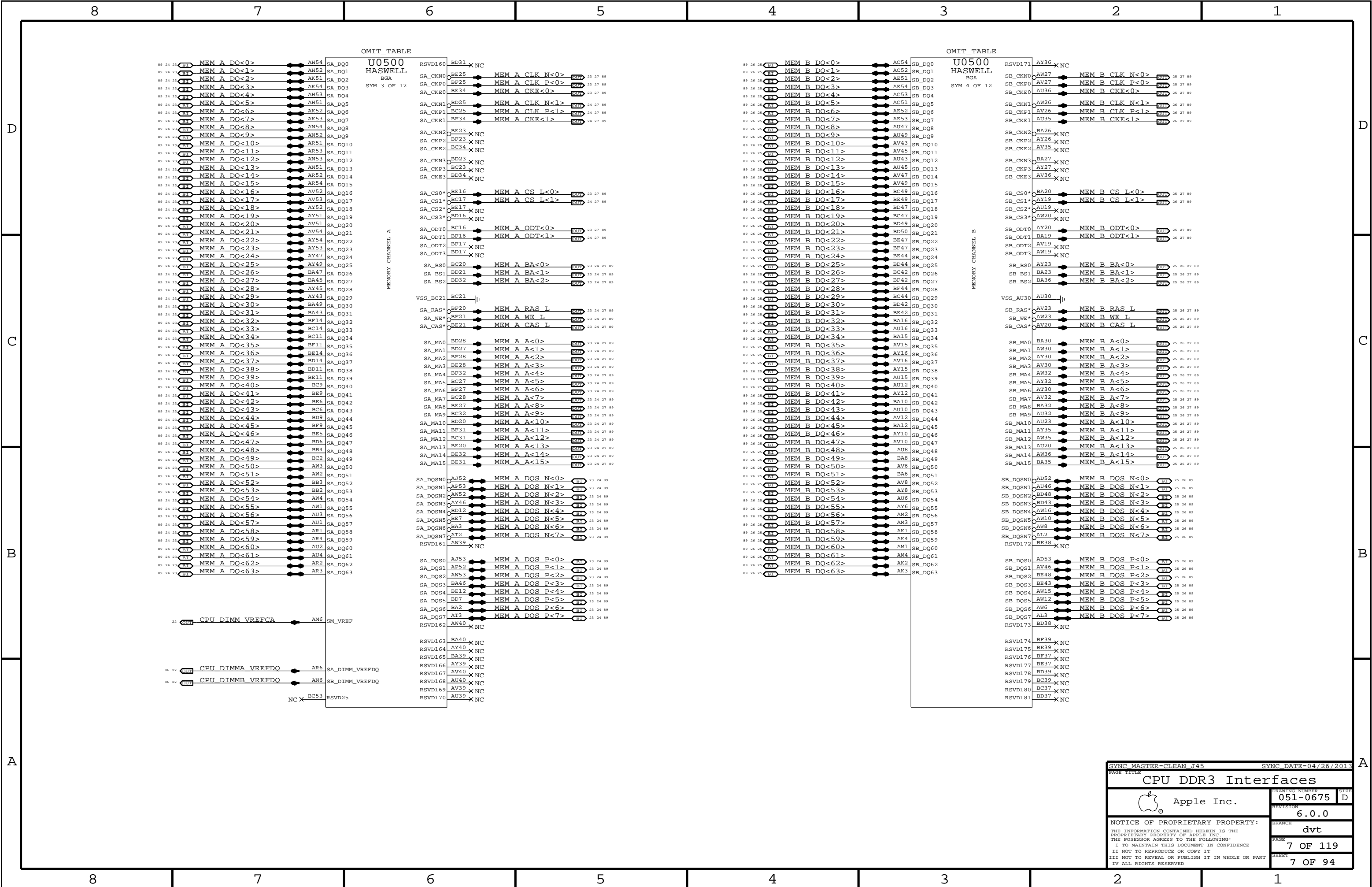


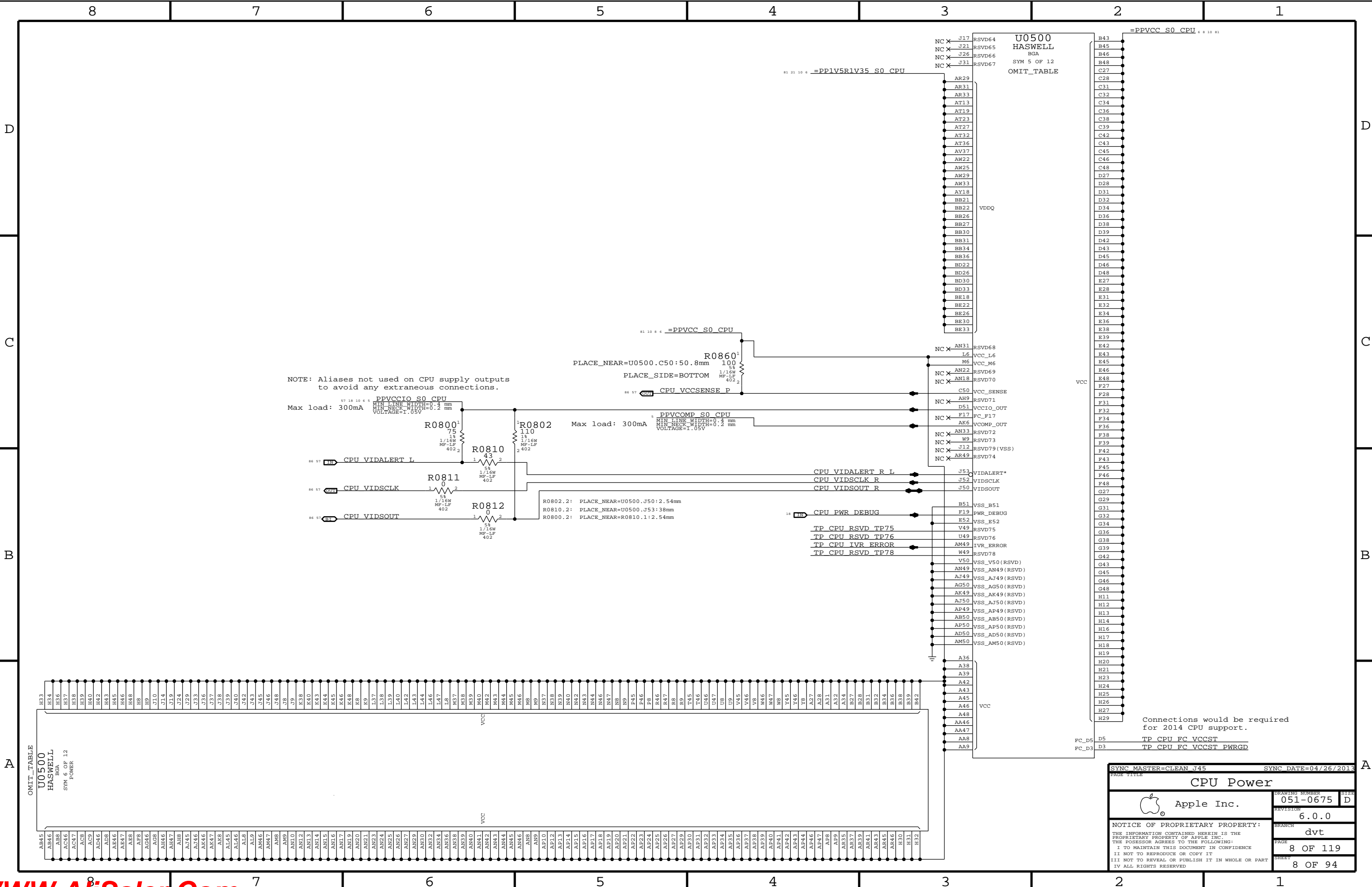
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NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

Max load: 300mA


PLACE\_NEAR=U0500.C50:50.8mm  
PLACE\_SIDE=BOTTOM

Max load: 300mA

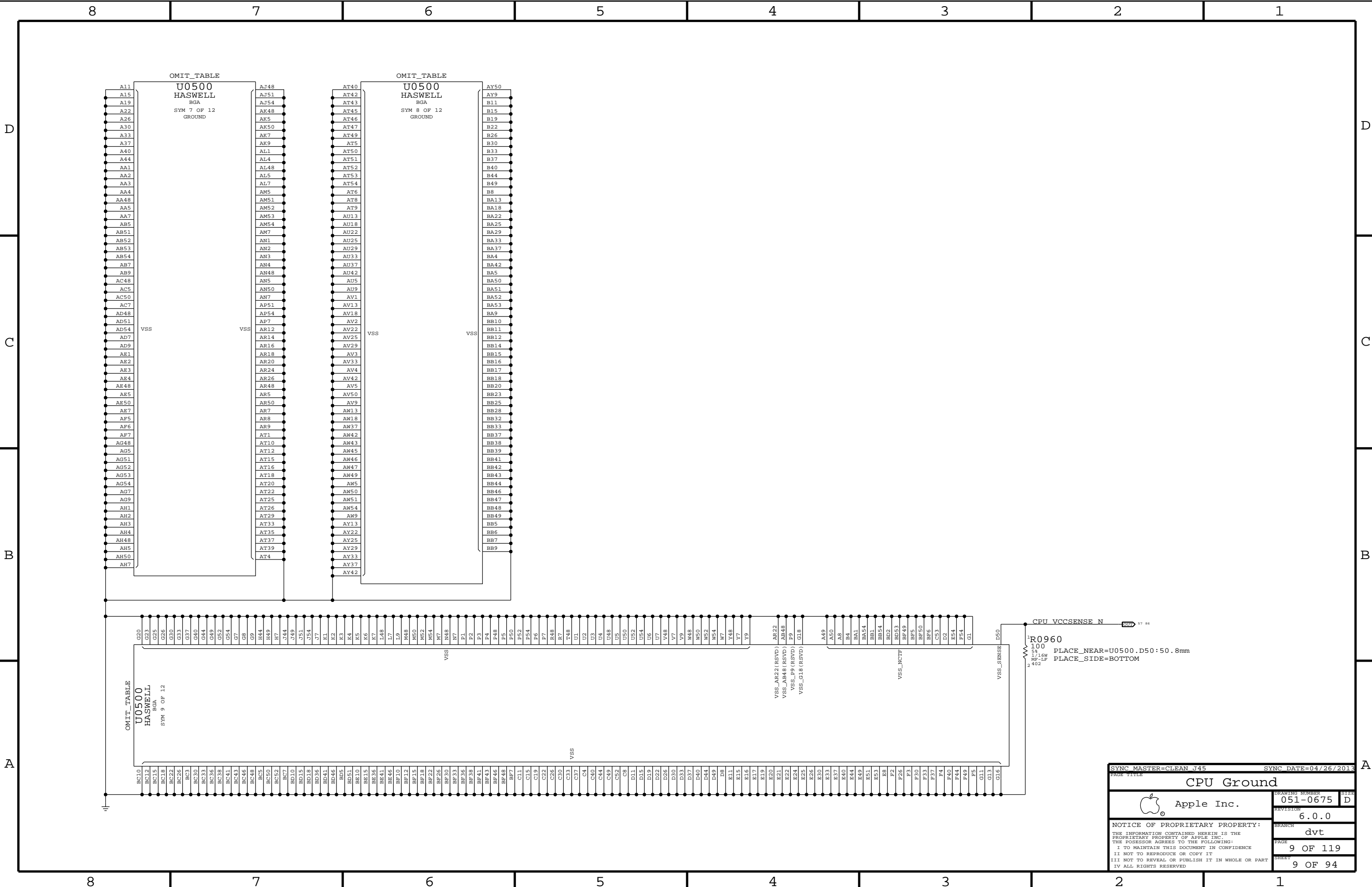
R0802.2: PLACE\_NEAR=U0500.J50:2.54mm  
R0810.2: PLACE\_NEAR=U0500.J53:38mm  
R0800.2: PLACE\_NEAR=R0810.1:2.54mm

Connections would be required for 2014 CPU support.

FC\_D5 D5 TP CPU FC VCCST  
FC\_D3 D3 TP CPU FC VCCST PWRGD

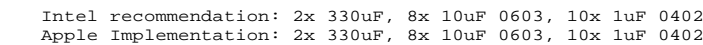
SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
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CPU Power			
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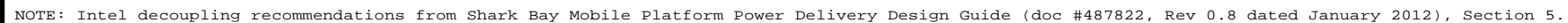
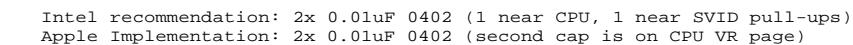



Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)  
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

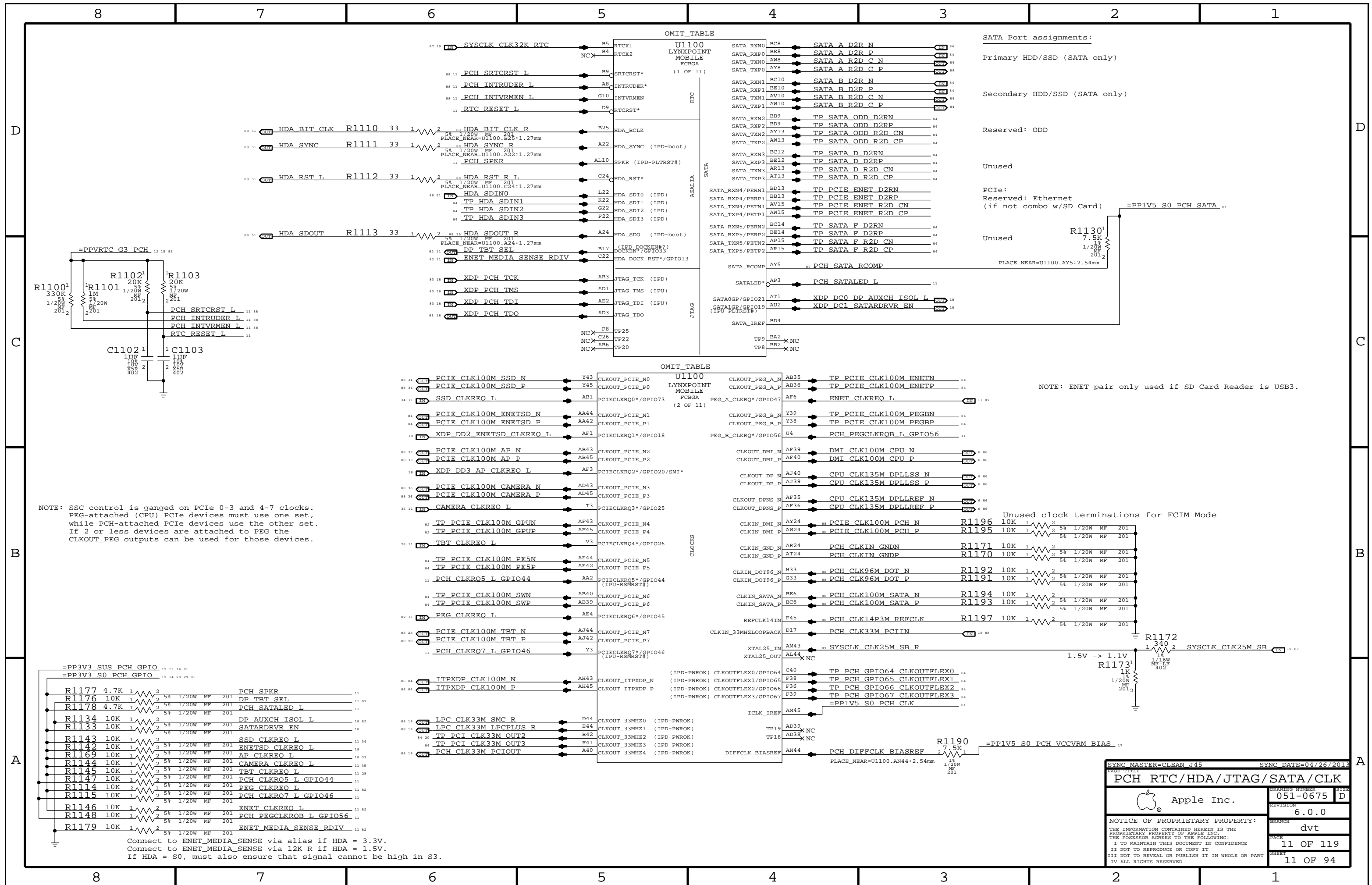
Place on bottom side of U0500



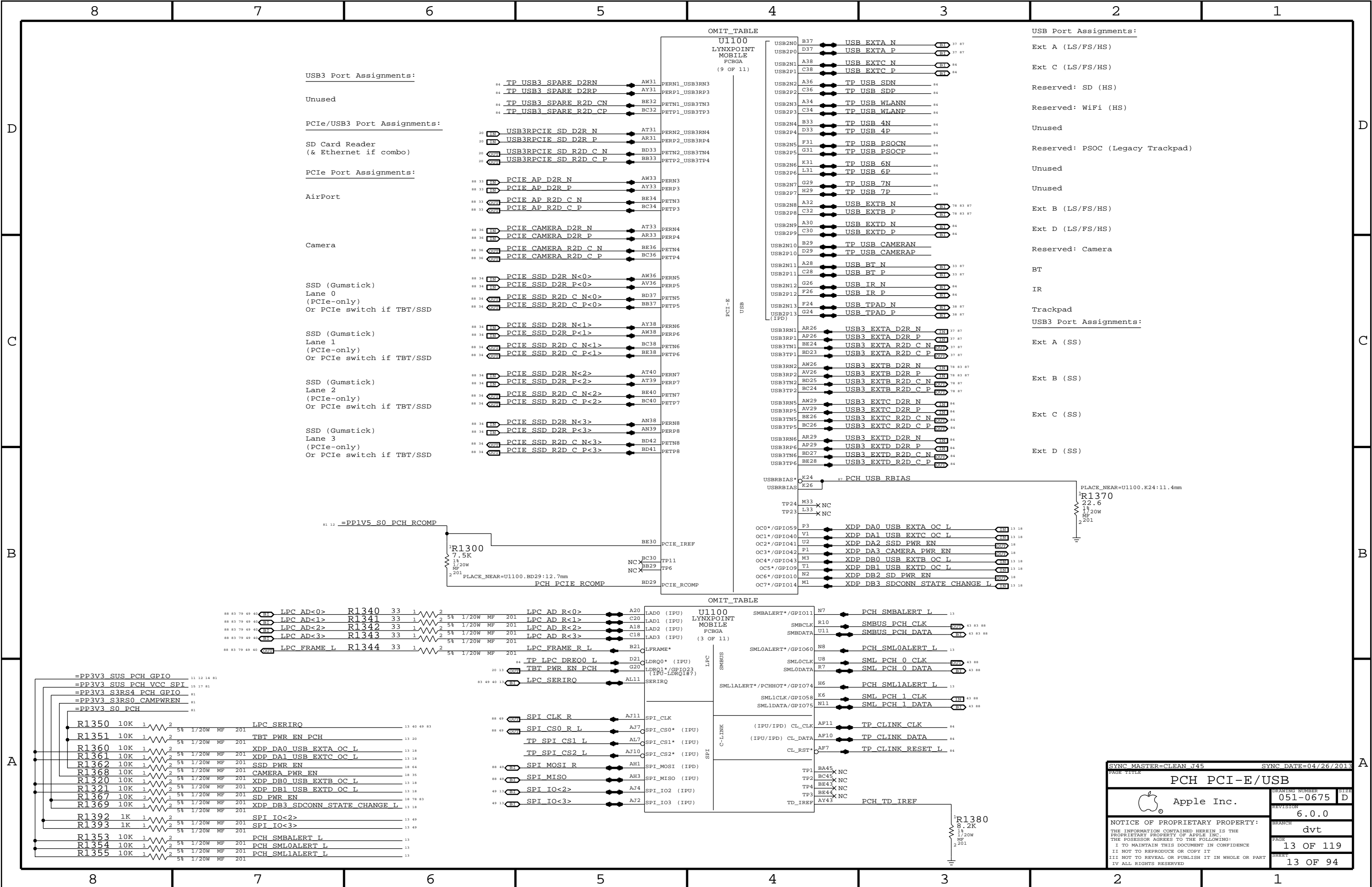
Place on bottom side of U0500

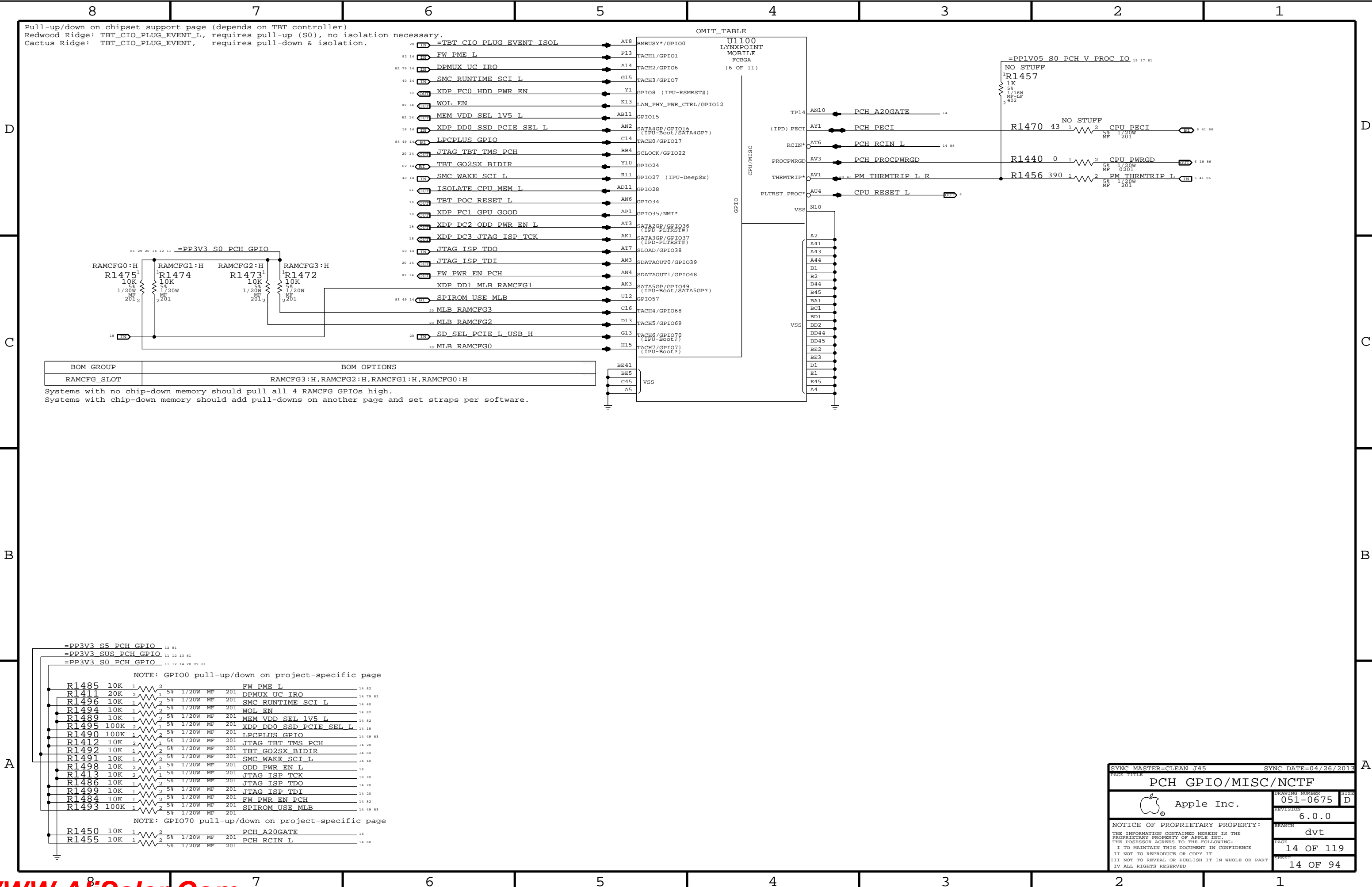


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CPU Decoupling			
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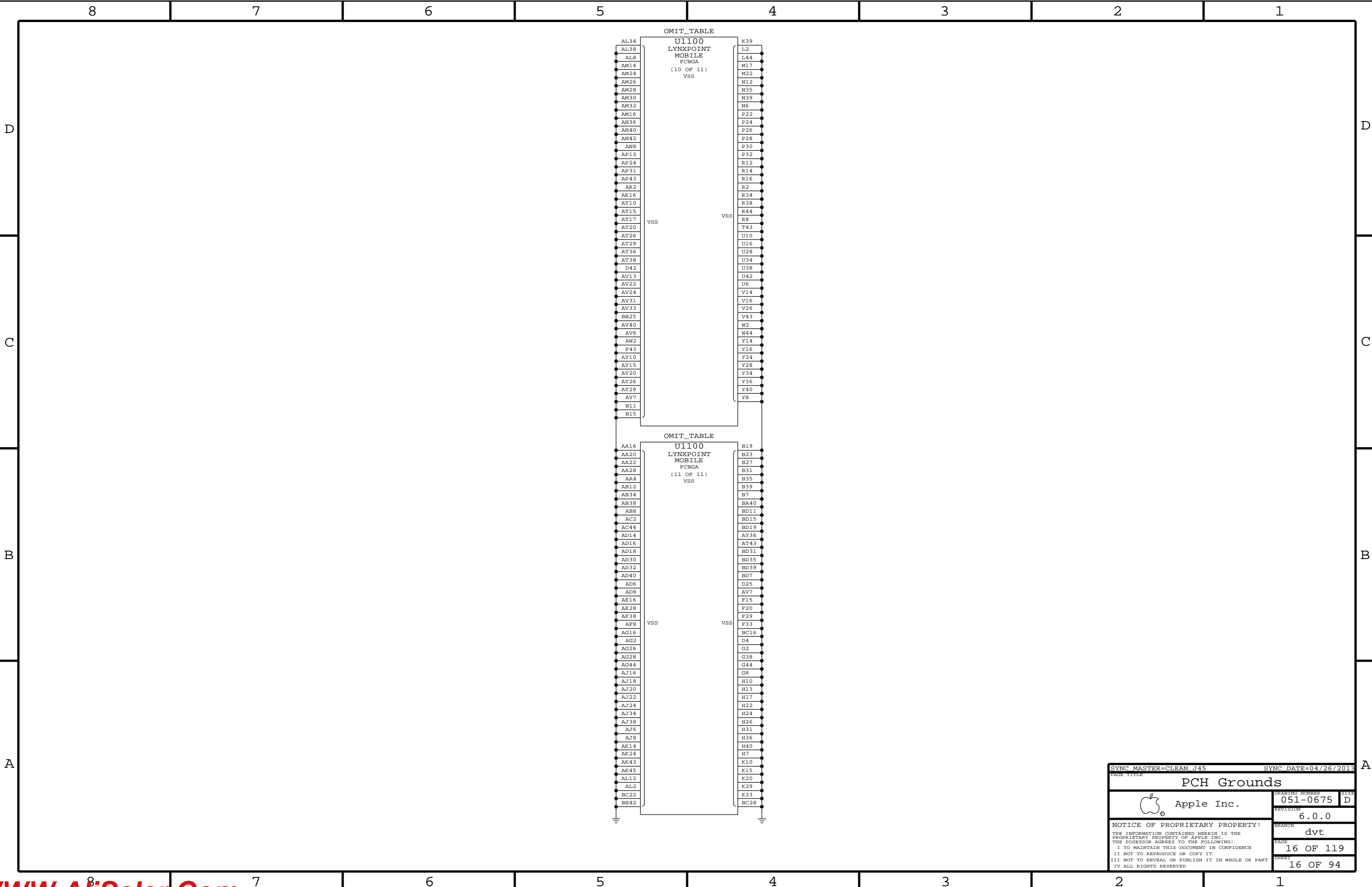













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SYNC DATE=04/26/2013

PCH Grounds

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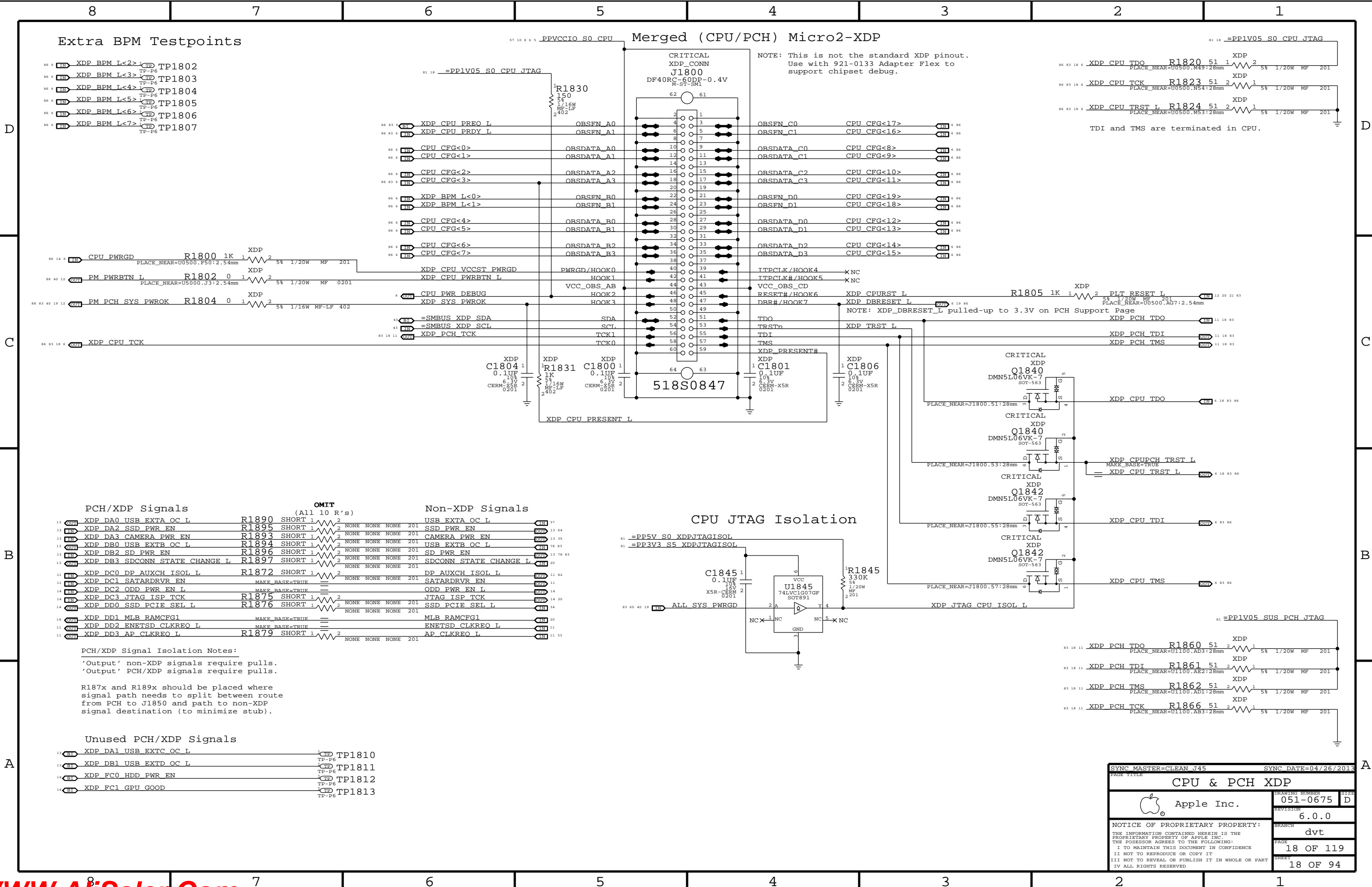
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Current data from LPT EDS (doc #486708, Rev 1.0).

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Extra BPM Testpoints

- XDP BPM L<2> TP1802
- XDP BPM L<3> TP1803
- XDP BPM L<4> TP1804
- XDP BPM L<5> TP1805
- XDP BPM L<6> TP1806
- XDP BPM L<7> TP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05 S0 CPU JTAG

- XDP CPU TDO R1820 51 1 2 5% 1/20W MF 201
- XDP CPU TCK R1823 51 2 2 5% 1/20W MF 201
- XDP CPU TRST L R1824 51 2 1 5% 1/20W MF 201

TDI and TMS are terminated in CPU.

PCH/XDP Signals

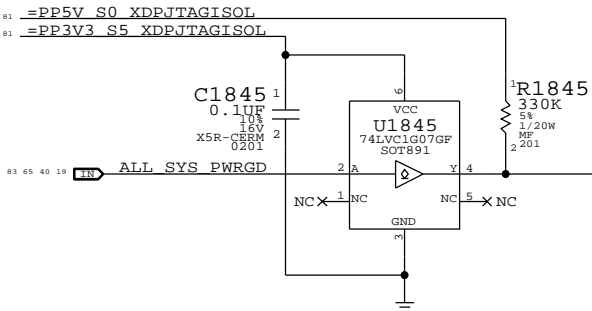
PCH/XDP Signals		Non-XDP Signals	
XDP DA0 USB EXTA OC L	R1890 SHORT 1 2	USB EXTA OC L	TP187
XDP DA2 SSD PWR EN	R1895 SHORT 1 2	SSD PWR EN	TP1834
XDP DA3 CAMERA PWR EN	R1893 SHORT 1 2	CAMERA PWR EN	TP1835
XDP DB0 USB EXTB OC L	R1894 SHORT 1 2	USB EXTB OC L	TP1878
XDP DB2 SD PWR EN	R1896 SHORT 1 2	SD PWR EN	TP1883
XDP DB3 SDCONN STATE CHANGE L	R1897 SHORT 1 2	SDCONN STATE CHANGE L	TP1870
XDP DC0 DP AUXCH ISOL L	R1872 SHORT 1 2	DP AUXCH ISOL L	TP1882
XDP DC1 SATARDVR EN	MAKE_BASE=TRUE	SATARDVR EN	TP1811
XDP DC2 ODD PWR EN L	MAKE_BASE=TRUE	ODD PWR EN L	TP1814
XDP DC3 JTAG ISP TCK	R1875 SHORT 1 2	JTAG ISP TCK	TP1820
XDP DD0 SSD PCIE SEL L	R1876 SHORT 1 2	SSD PCIE SEL L	TP1814
XDP DD1 MLB RAMCFG1	MAKE_BASE=TRUE	MLB RAMCFG1	TP1820
XDP DD2 ENETSD CLKREQ L	MAKE_BASE=TRUE	ENETSD CLKREQ L	TP1811
XDP DD3 AP CLKREQ L	R1879 SHORT 1 2	AP CLKREQ L	TP1813

PCH/XDP Signal Isolation Notes:  
'Output' non-XDP signals require pulls.  
'Output' PCH/XDP signals require pulls.  
  
R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

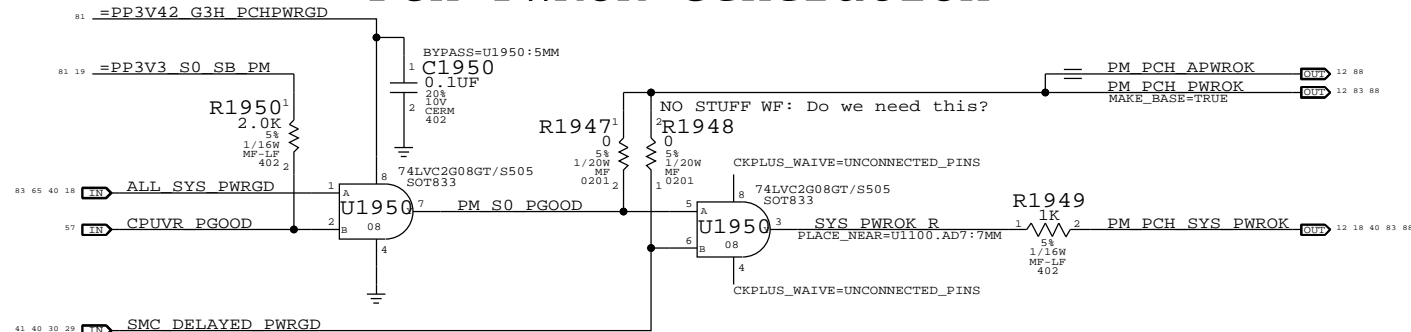
- XDP DA1 USB EXTC OC L TP1810
- XDP DB1 USB EXTD OC L TP1811
- XDP FC0 HDD PWR EN TP1812
- XDP FC1 GPU GOOD TP1813

CPU JTAG Isolation



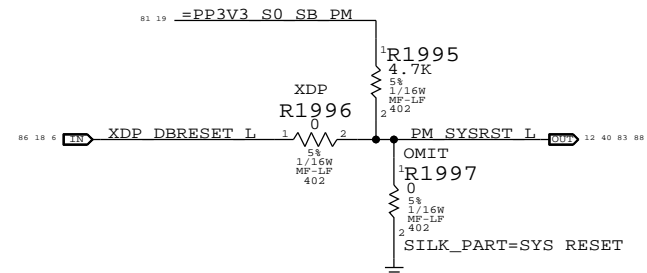
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CPU & PCH XDP		DRAWING NUMBER	
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# PCH PWROK Generation



NOTE: ALL\_SYS\_PWRGD must remain low until at least 5ms after all rails are valid.

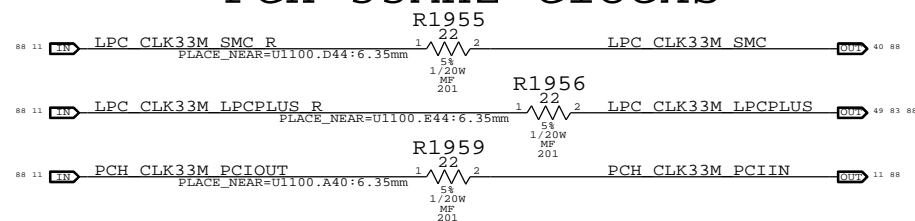
## PCH Reset Button



## PCH ME Disable Strap

PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH 33MHz Clocks



## System RTC Power Source &amp; 32kHz / 25MHz Clock Generator

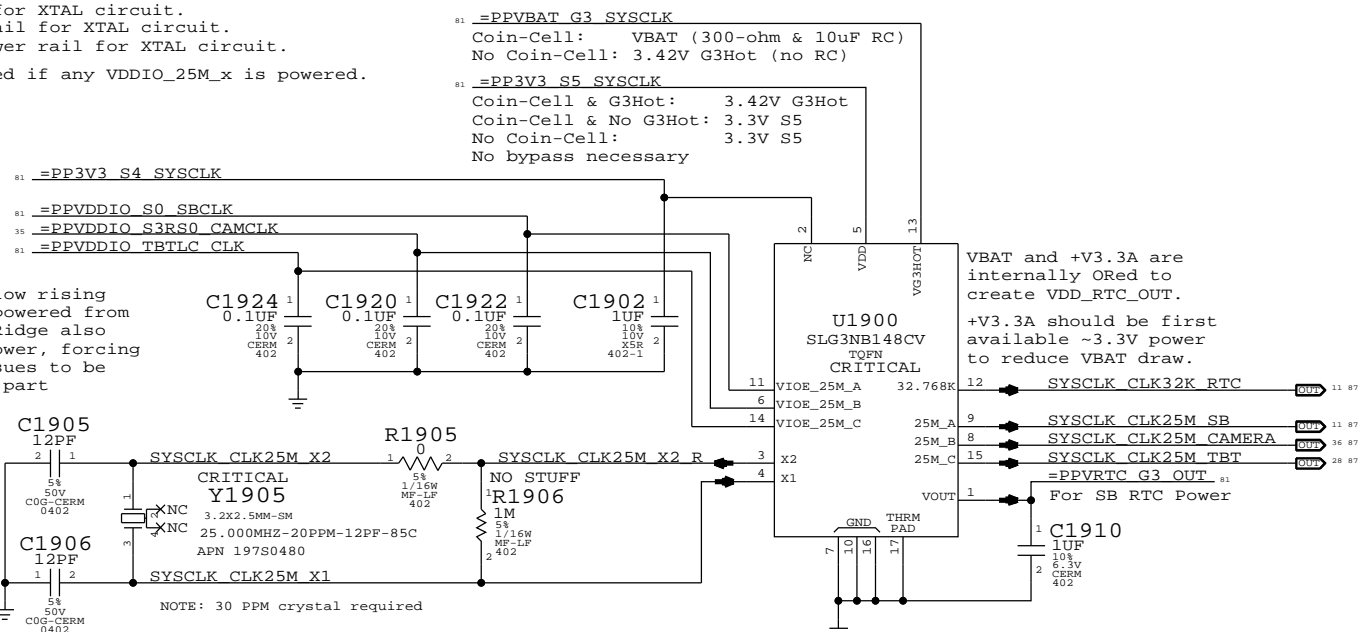
VDDIO\_25M\_A: SB power rail for XTAL circuit.  
VDDIO\_25M\_B: Camera power rail for XTAL circuit.  
VDDIO\_25M\_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD\_25M must be powered if any VDDIO\_25M\_x is powered.

GreenClk 25MHz Power


```
SB XTAL Power
Camera XTAL Power
TBT XTAL Power
```

NOTE: SLG3NB148A provides slow rising edge on 25MHZ\_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD\_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



VBAT and +V3.3A are internally ORed to create VDD\_RTC\_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

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Chipset Support		DRAWING NUMBER	
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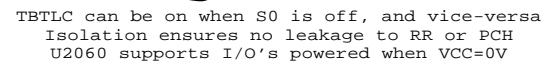
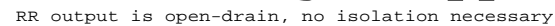
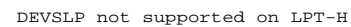
## D



SD Card Reader is always USB3 in this implementaton.

B

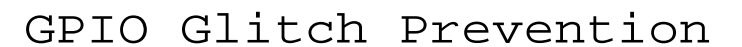
## A




## D



## B



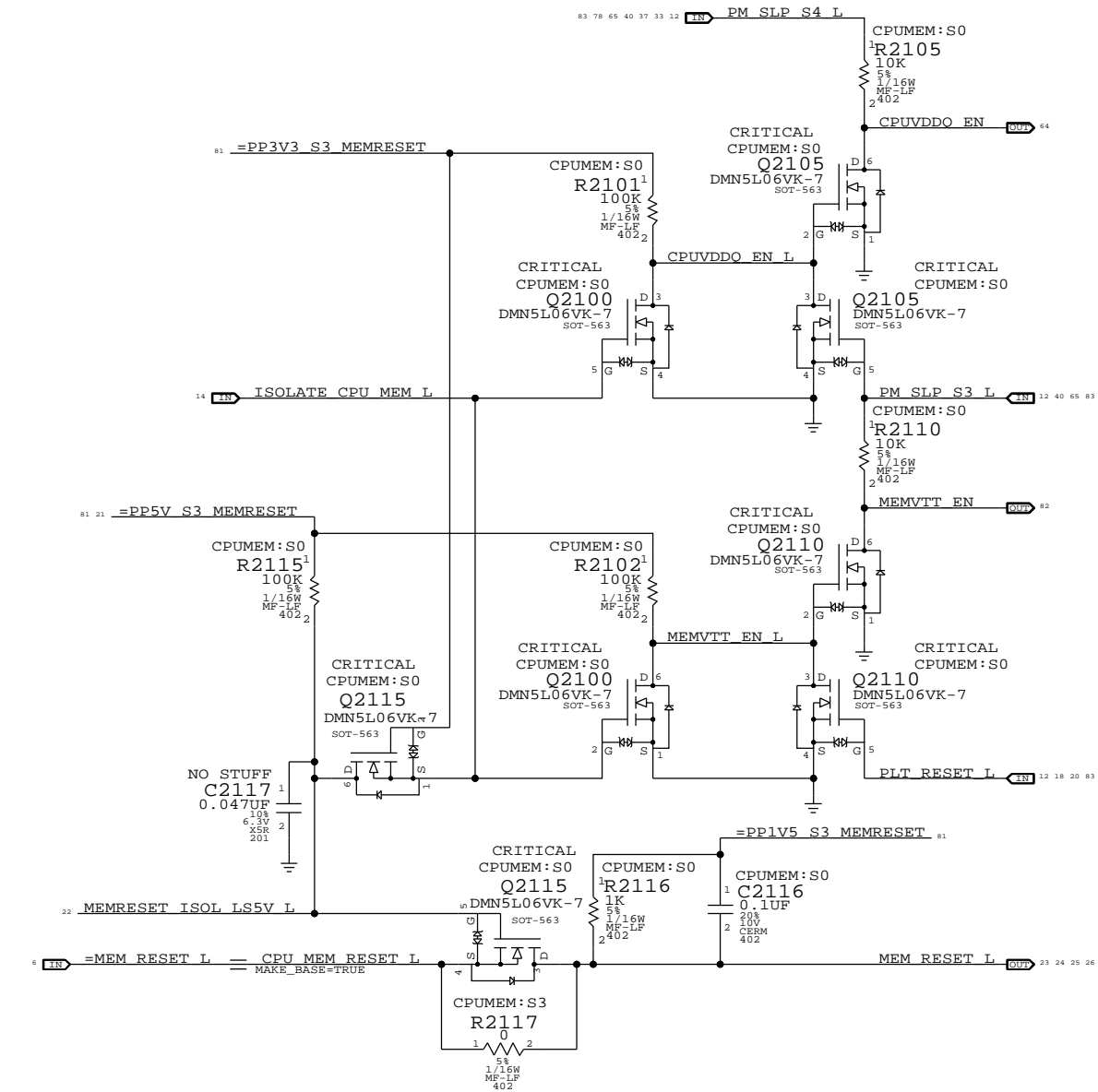
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Project Chipset Support			
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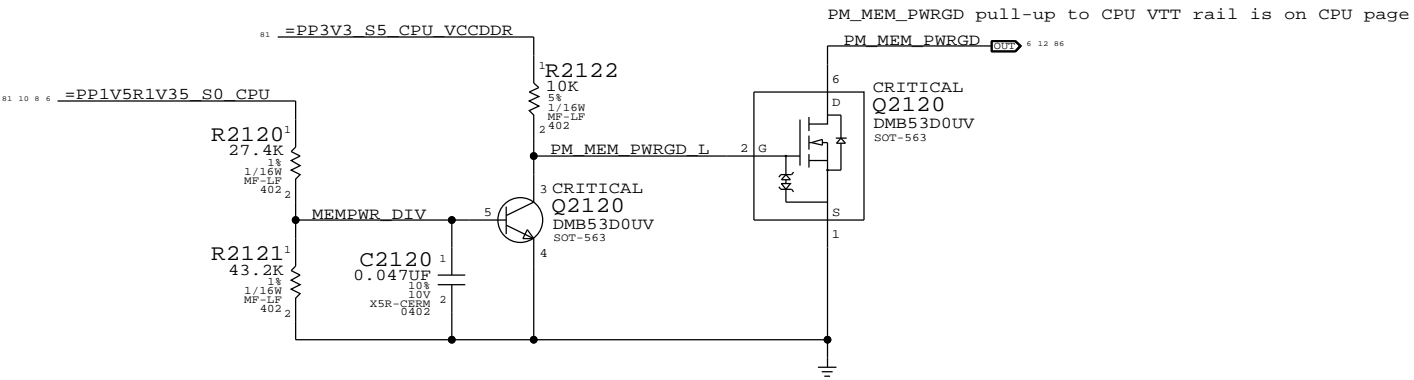
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3<->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

CPUVDDQ\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

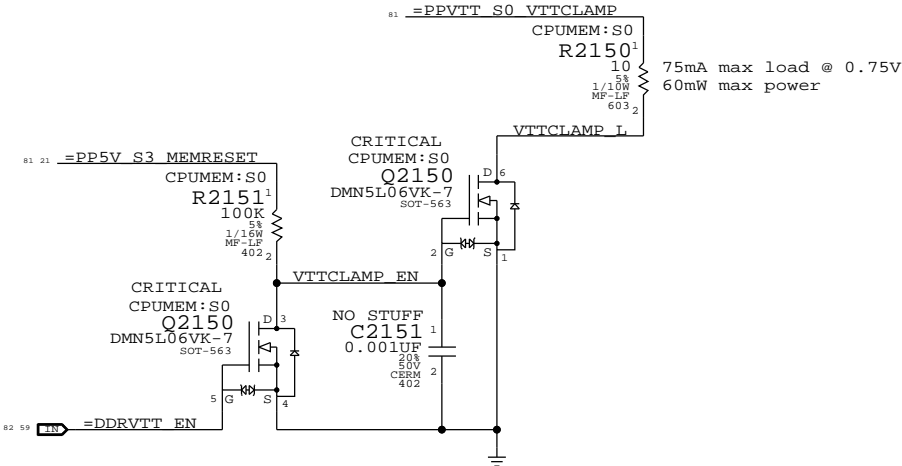


MEM S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

PAGE TITLE		SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
CPU Memory S3 Support		DRAWING NUMBER		051-0675	
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Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN  
- =PPDDR\_S3\_MEMVREF

Signal aliases required by this page:

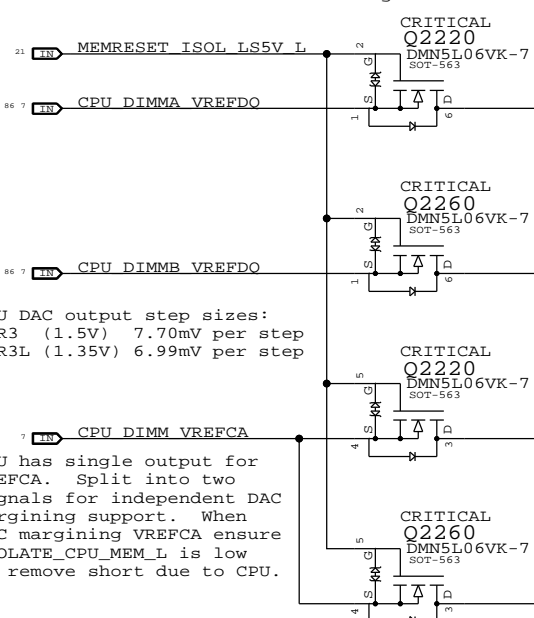
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- DDRVREF\_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

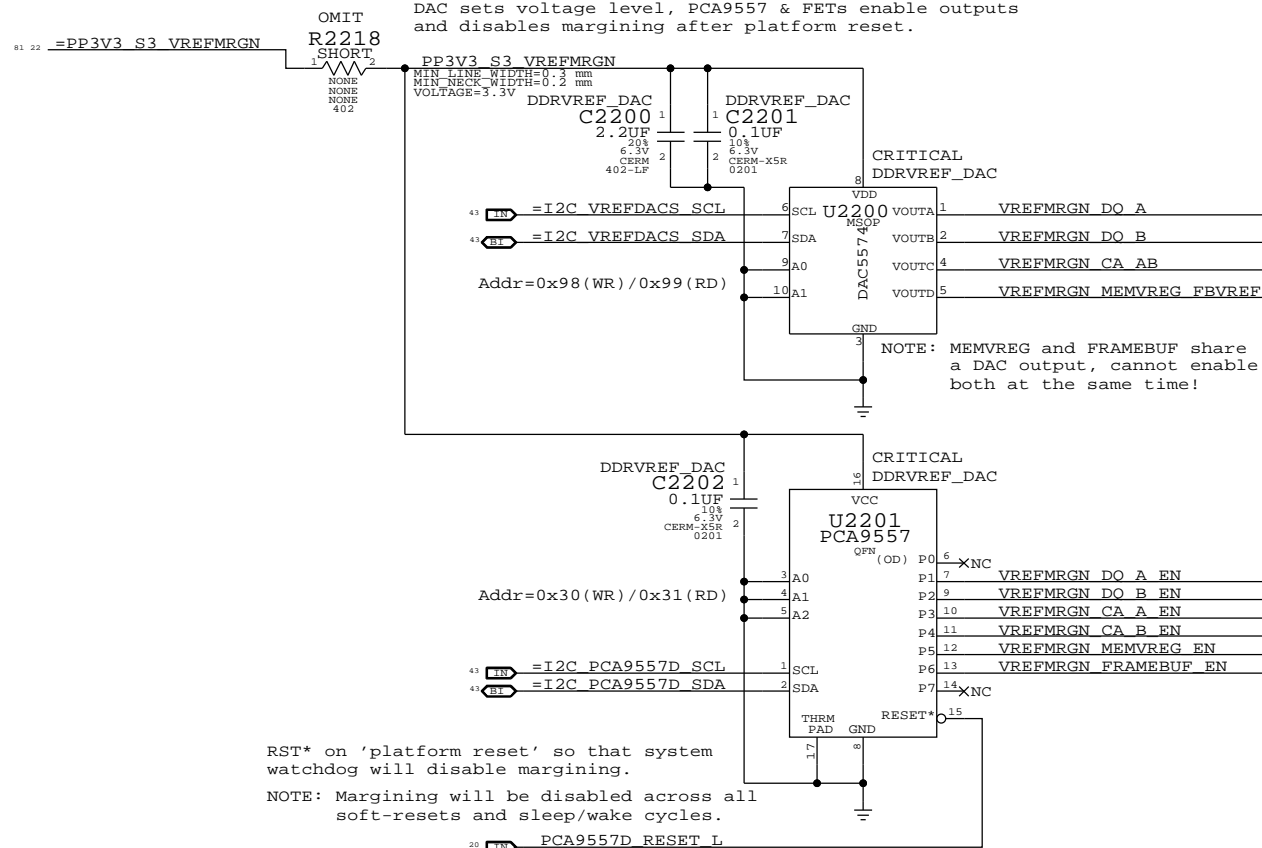


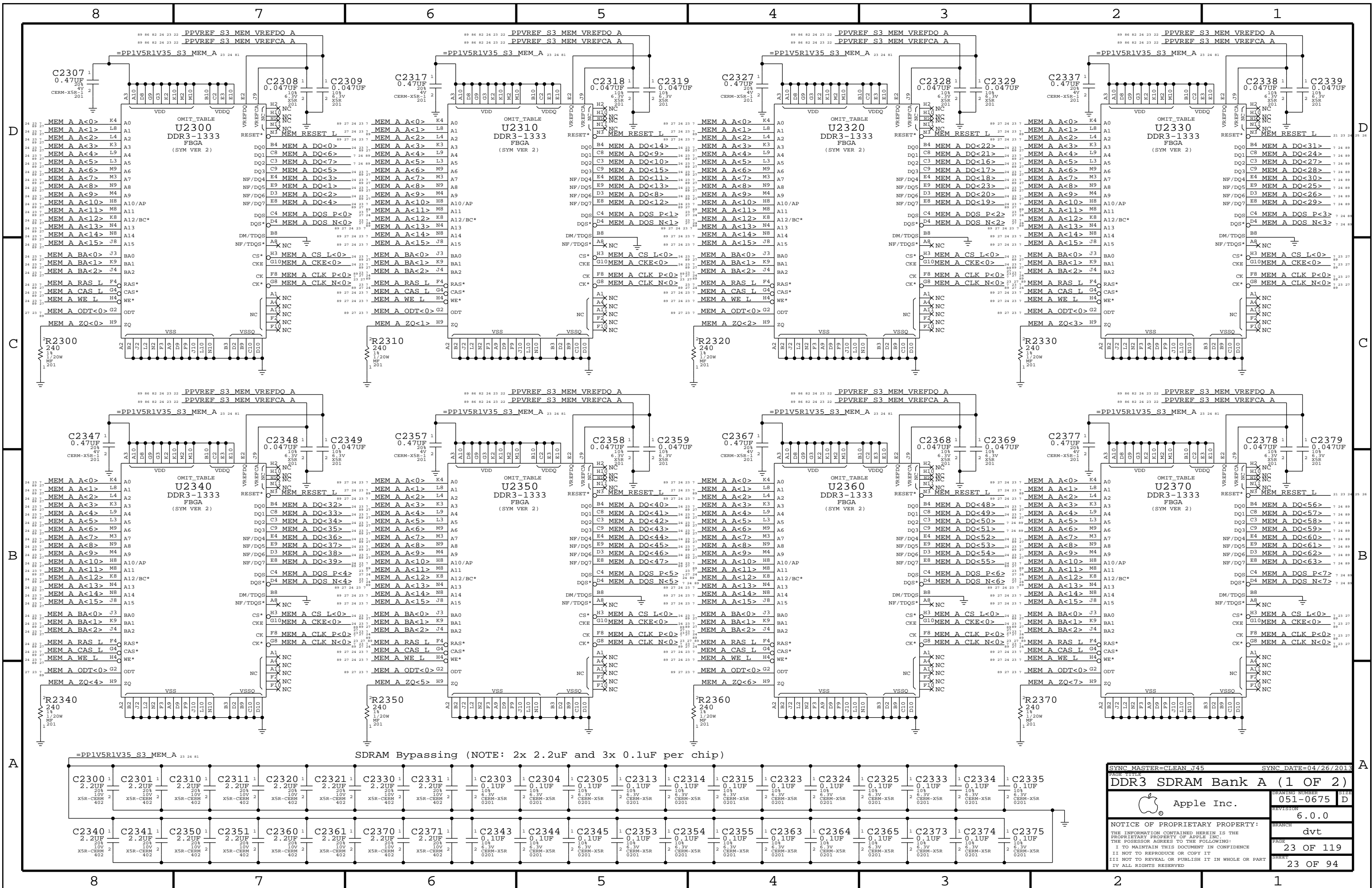
NOTE: CPU DAC output step sizes:  
DDR3 (1.5V) 7.70mV per step  
DDR3L (1.35V) 6.99mV per step

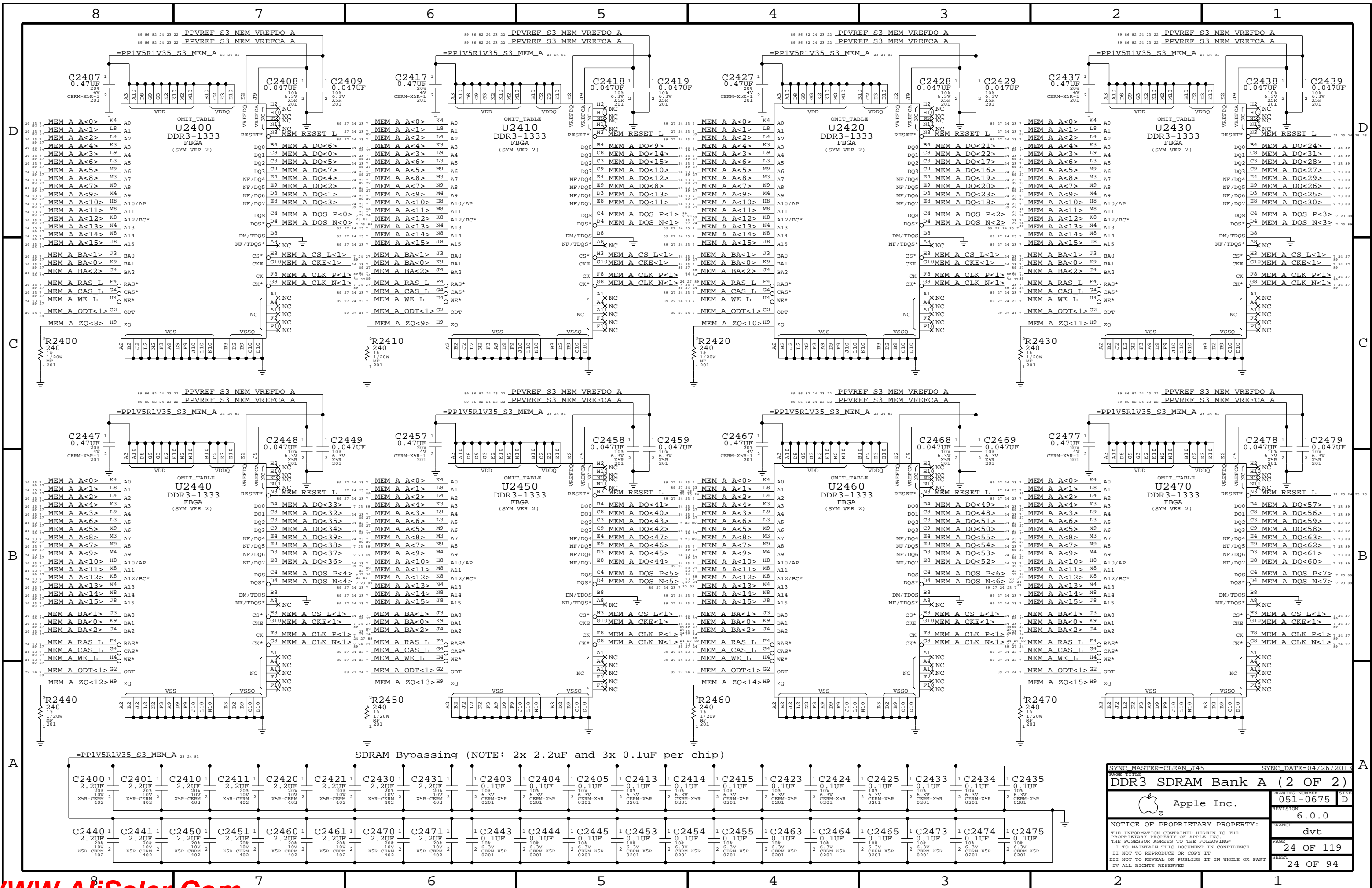
NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE\_CPU\_MEM\_L is low to remove short due to CPU.

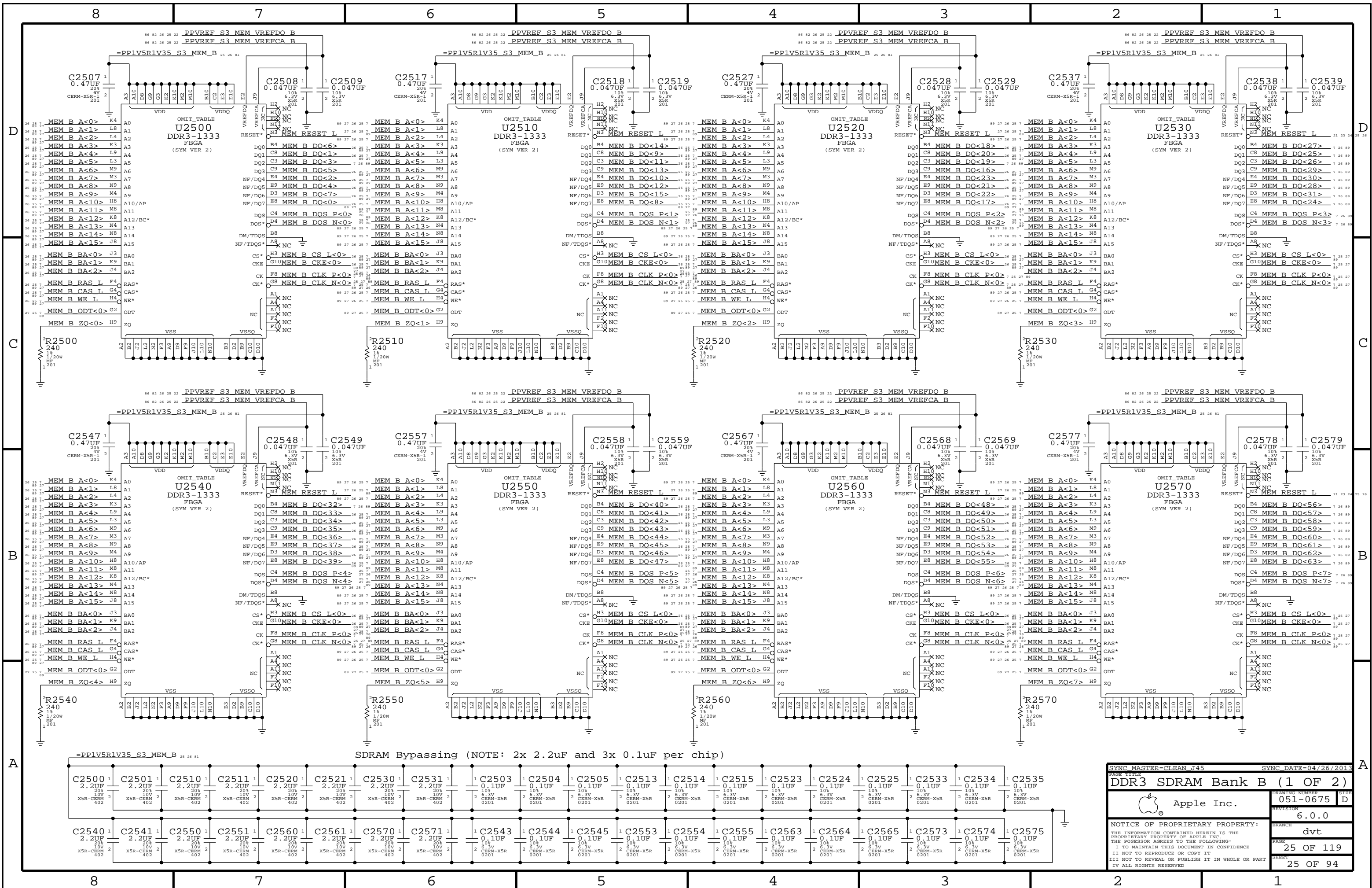
DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.







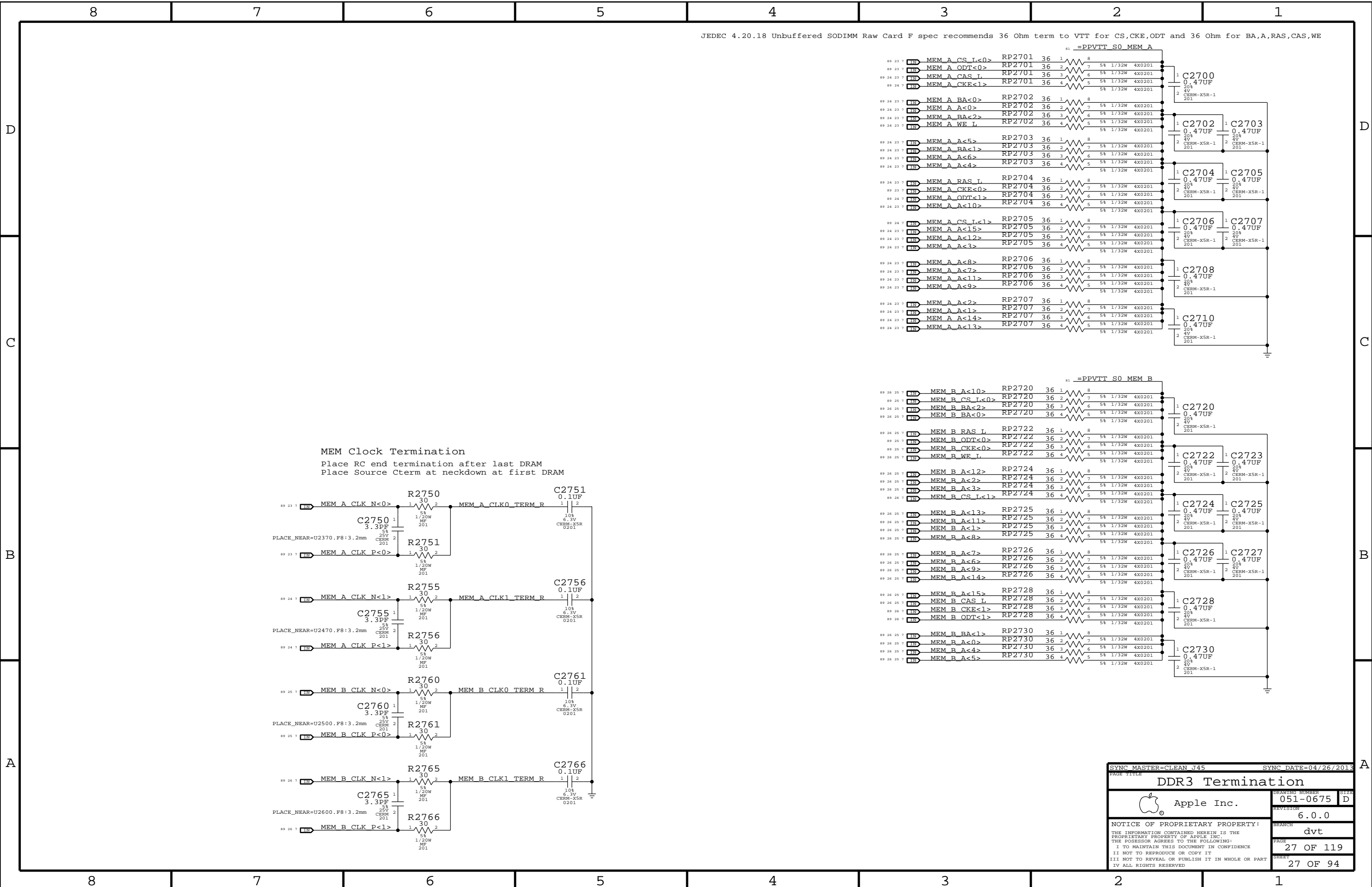


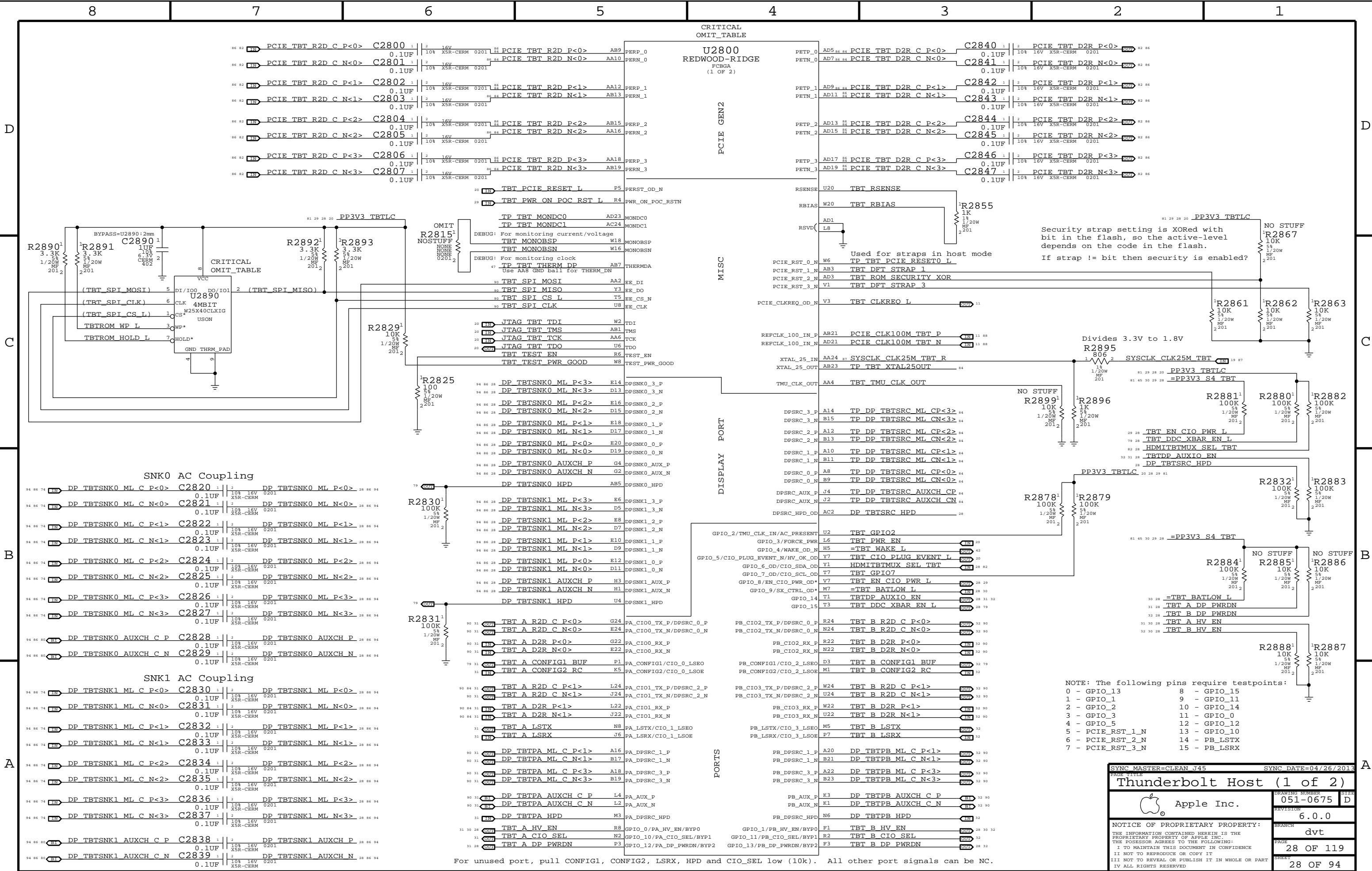
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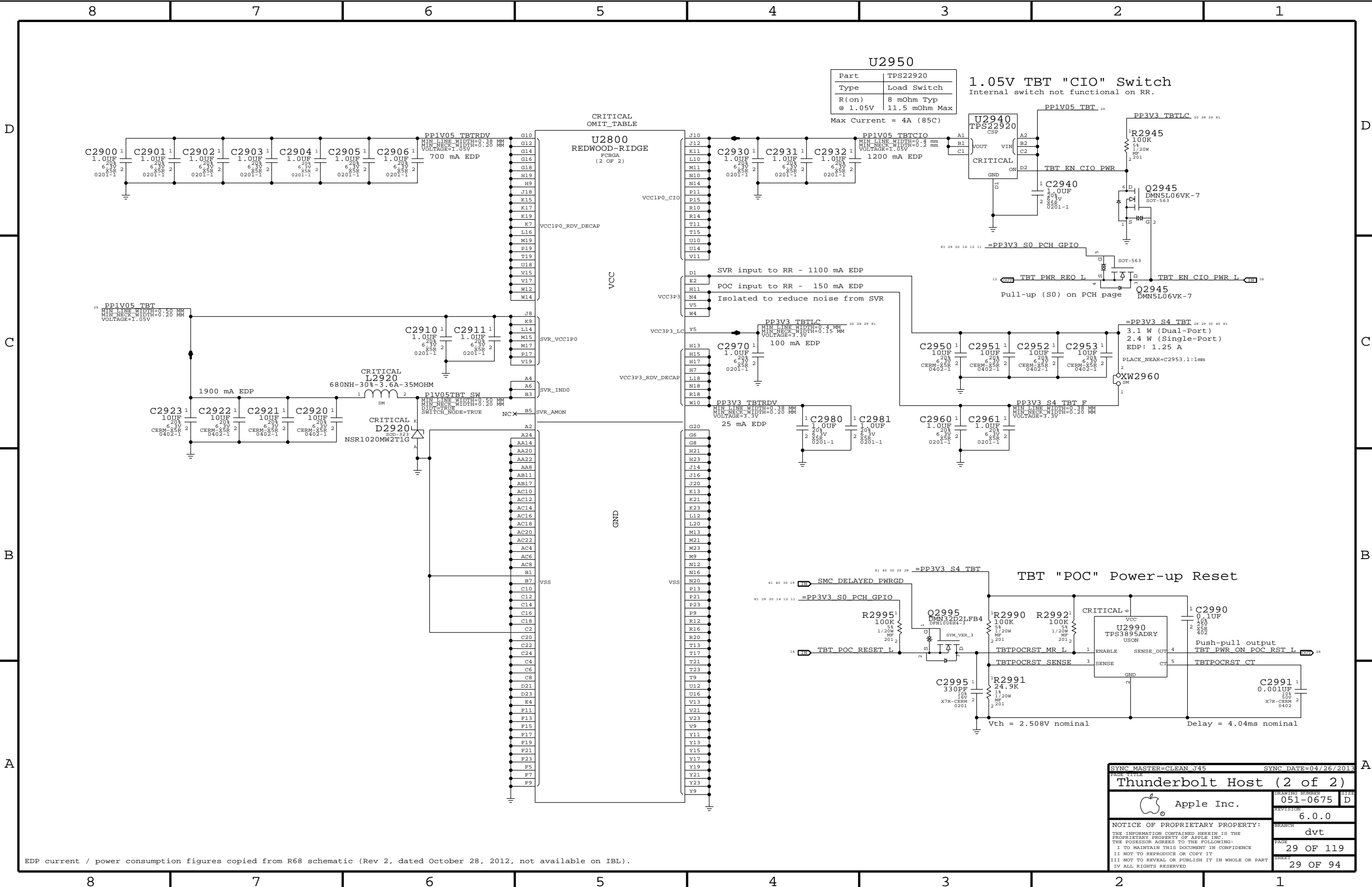













EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch

Internal switch not functional on RR.

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PAGE TITLE		Thunderbolt Host (2 of 2)	
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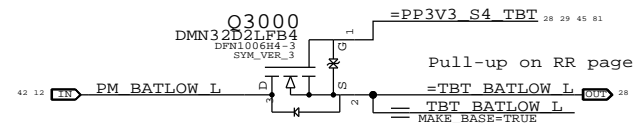
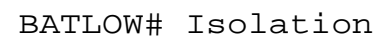
Power aliases required by this page:  
- =PPVIN\_SW\_TBTBST (8-13V Boost Input)  
- =PP15V\_TBT\_REG (15V Boost Output)


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Signal aliases required by this page:  
(NONE)

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BOM options provided by this page:  
(NONE)



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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

B

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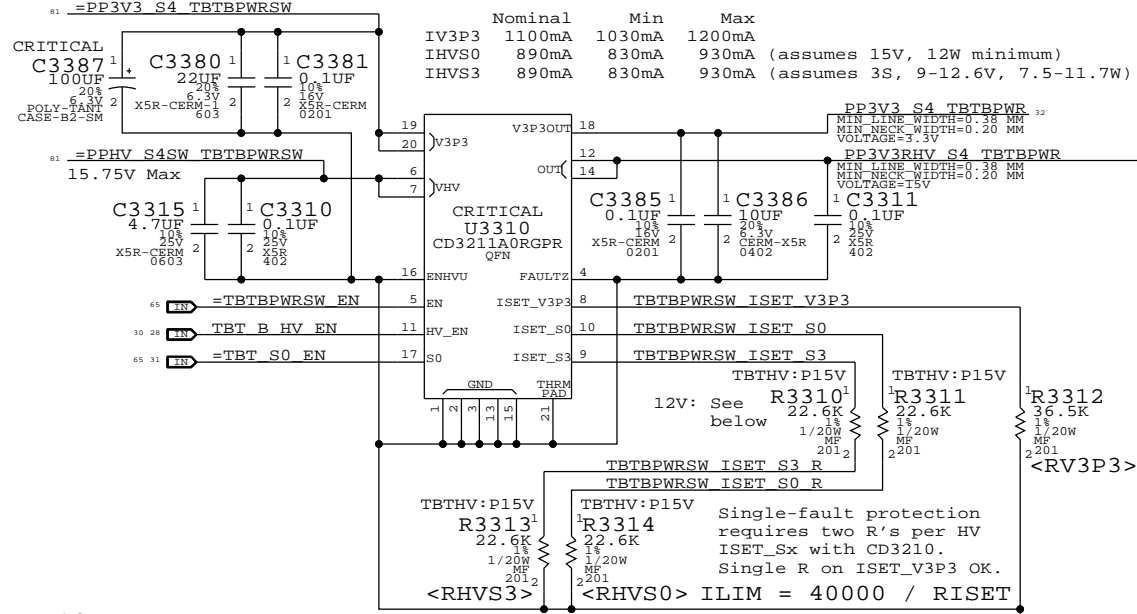


A



## 3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

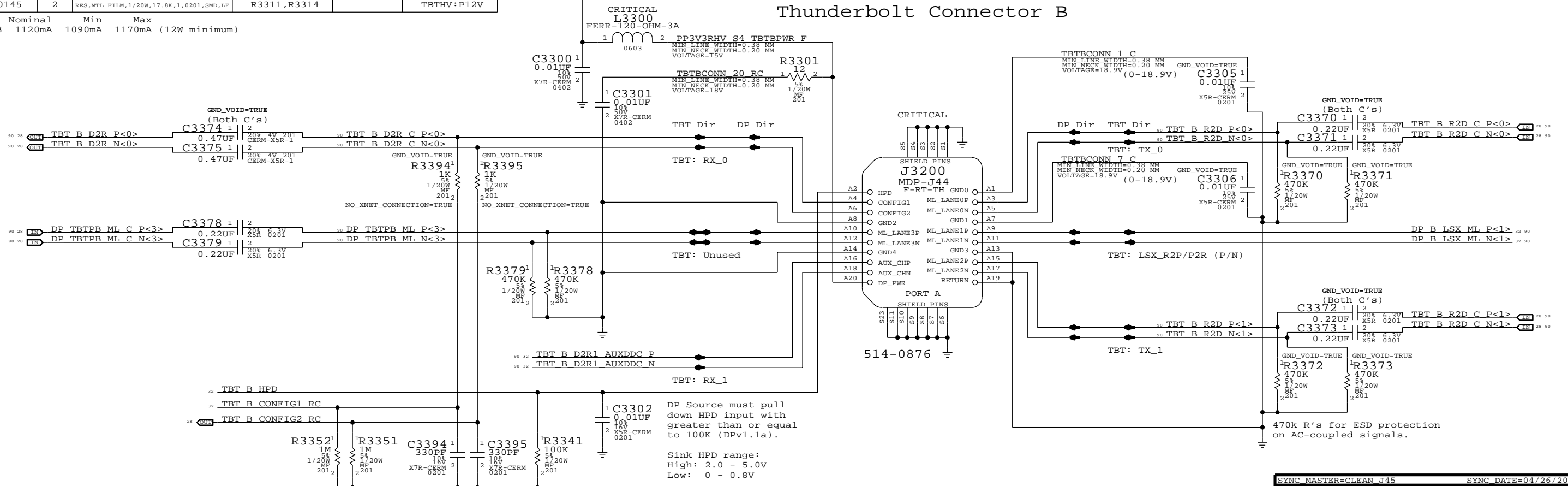



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

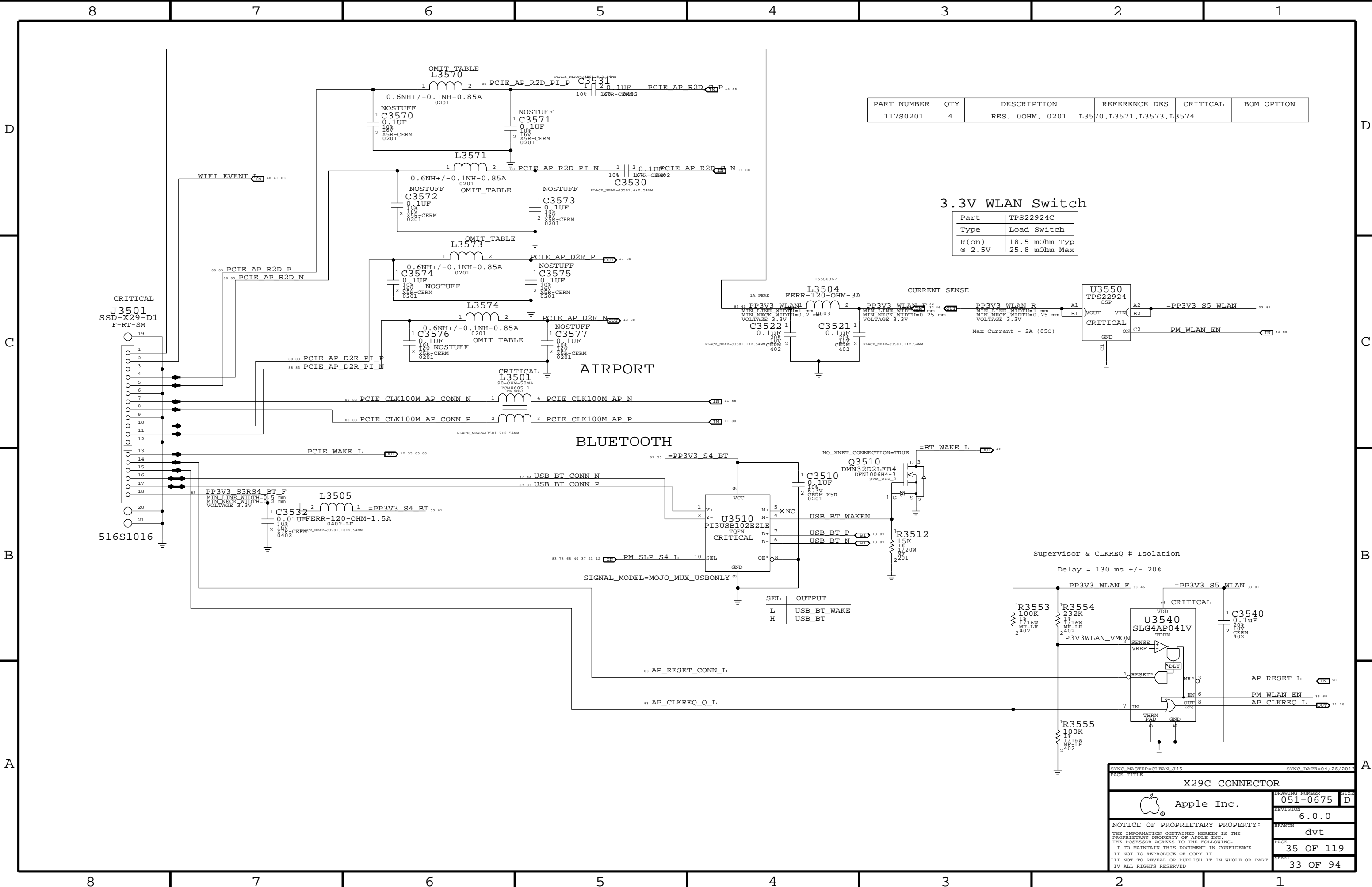
Nominal Min Max  
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

## Thunderbolt Connector B



SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
Thunderbolt Connector B			
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		SIZE	D
		REVISION	6.0.0
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




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 00HM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
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X29C CONNECTOR		DRAWING NUMBER	
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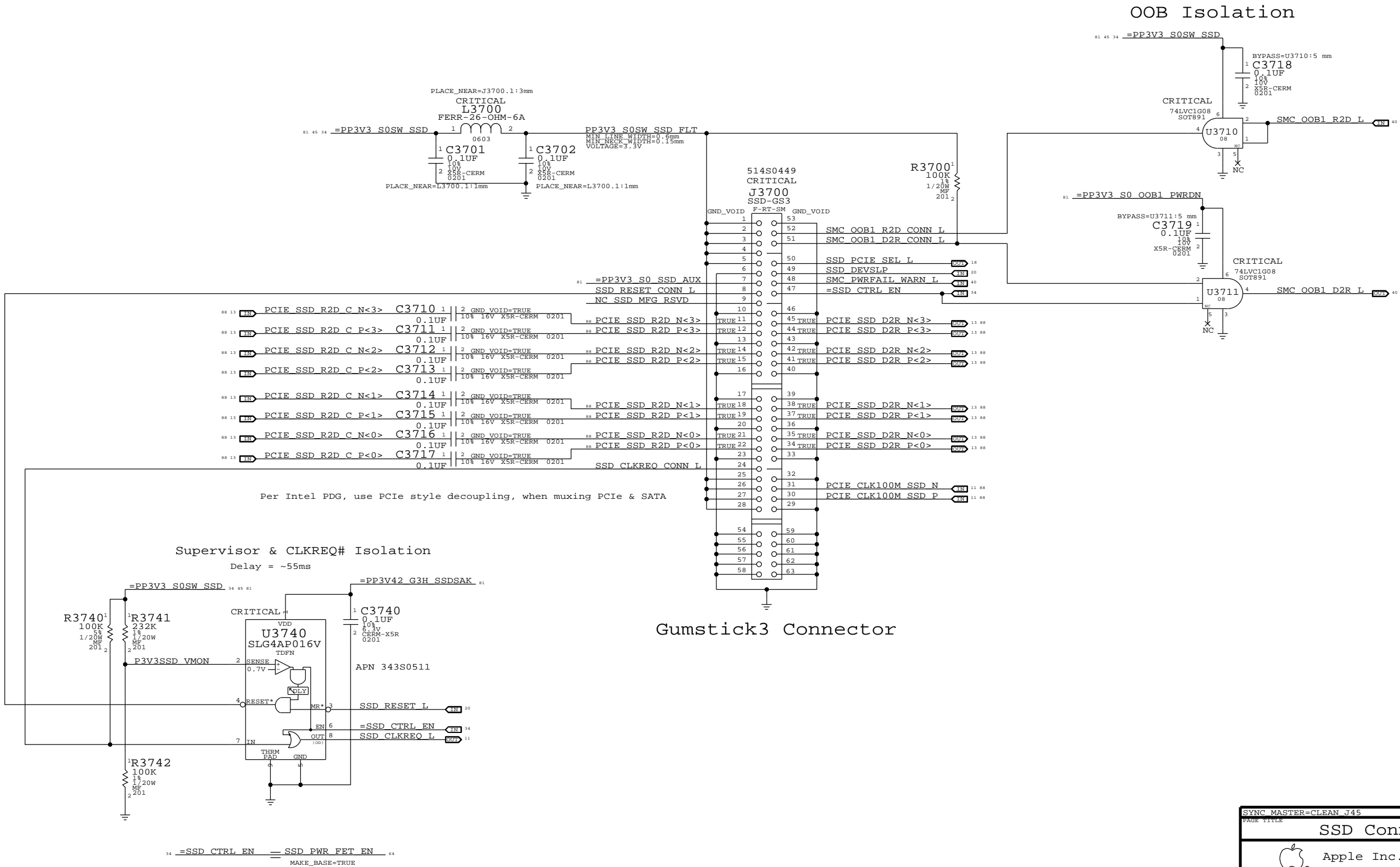
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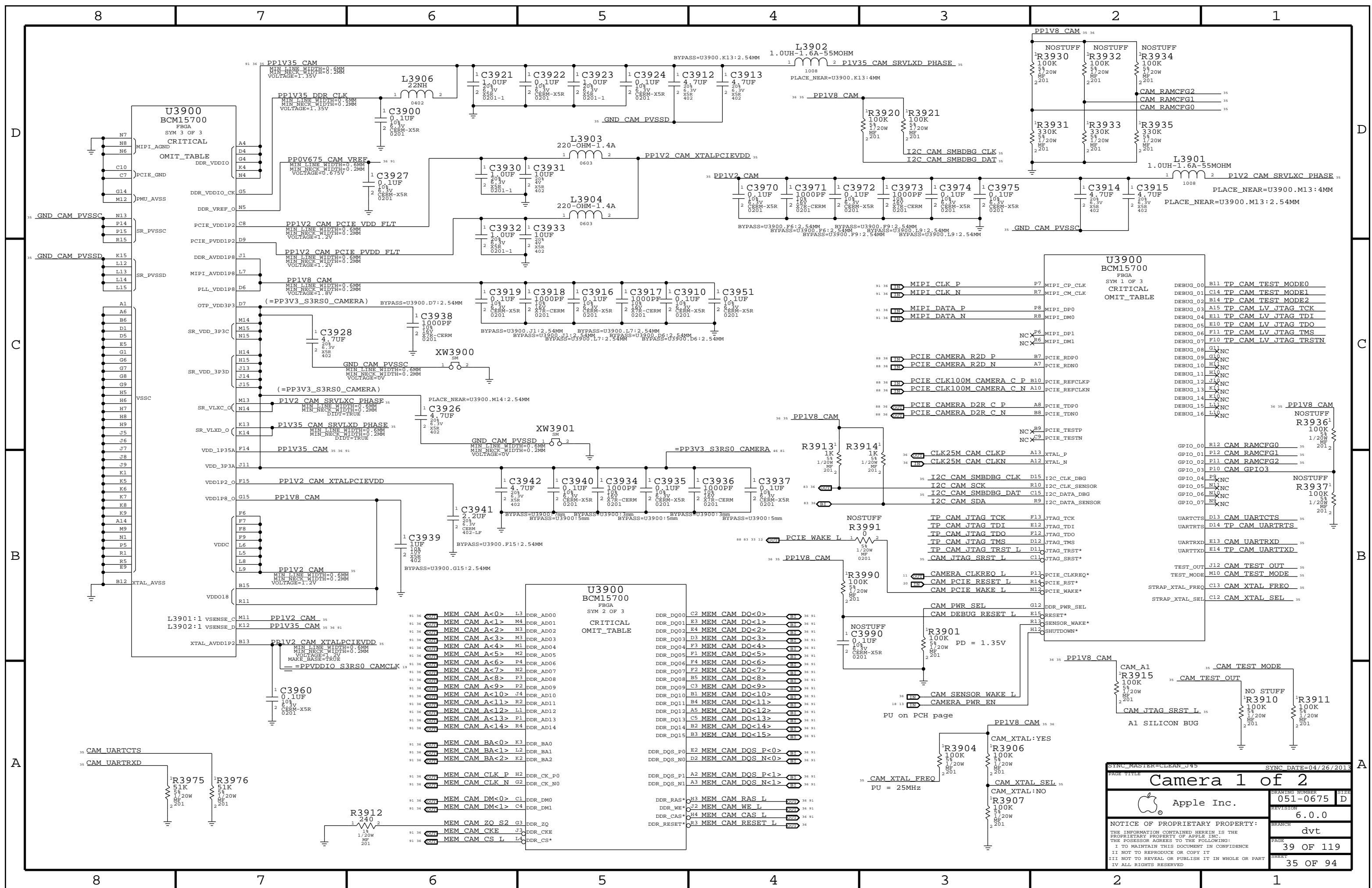
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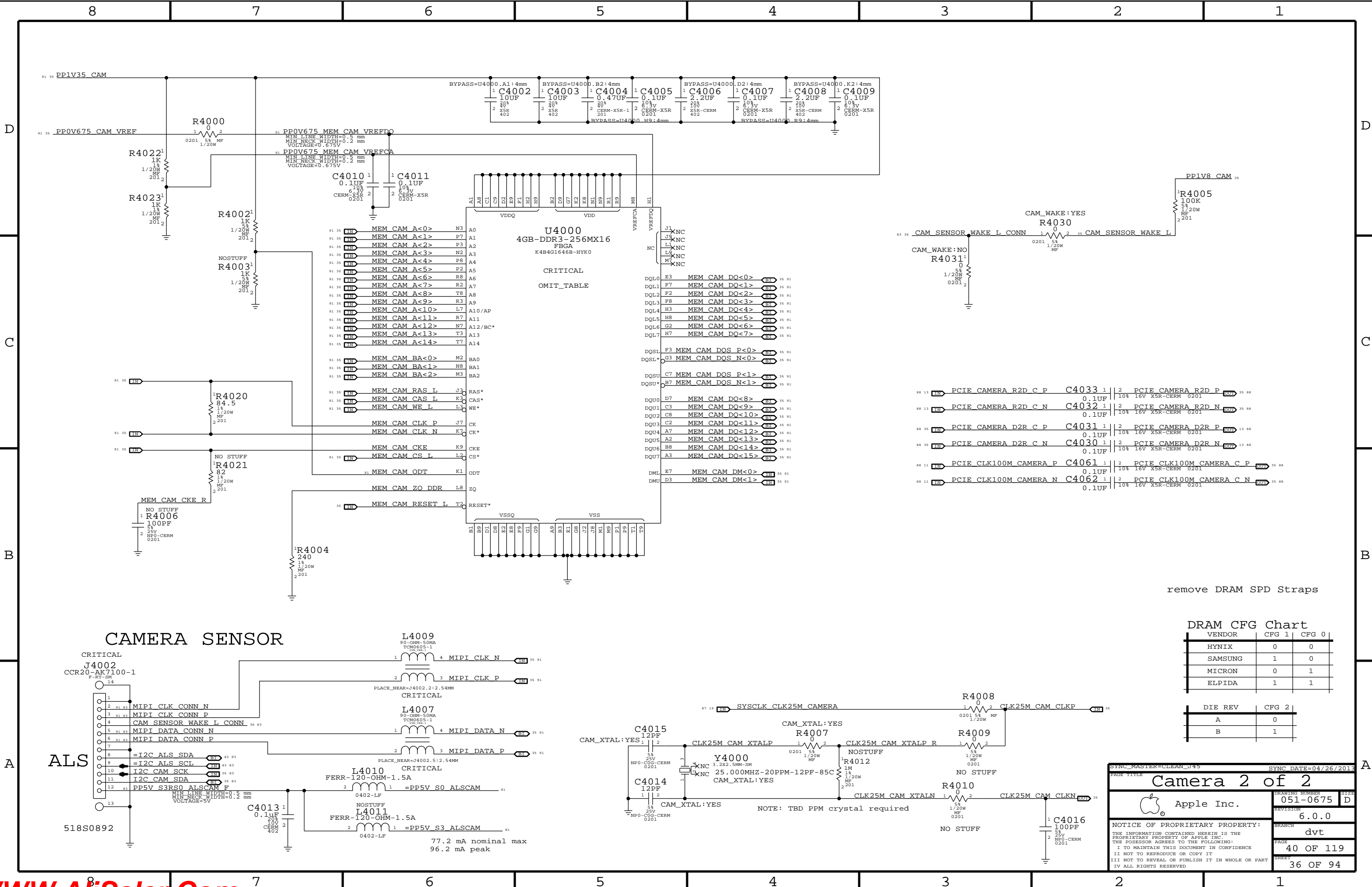
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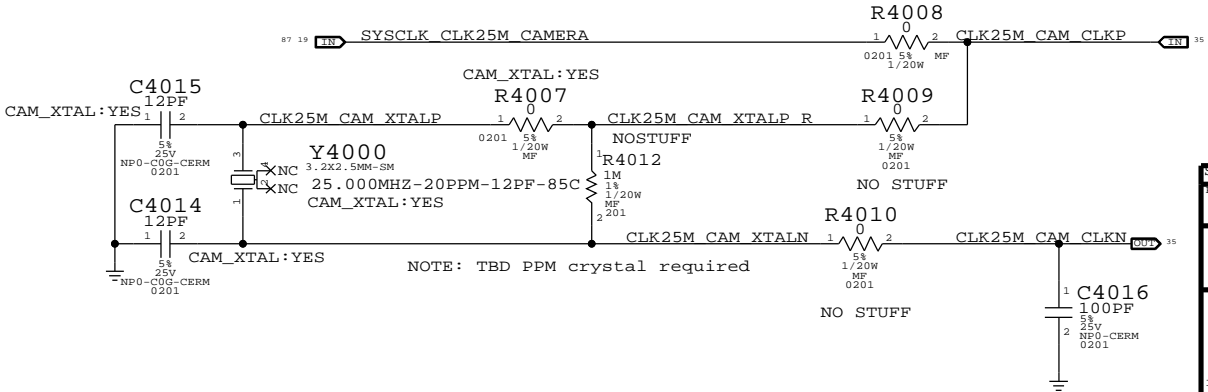
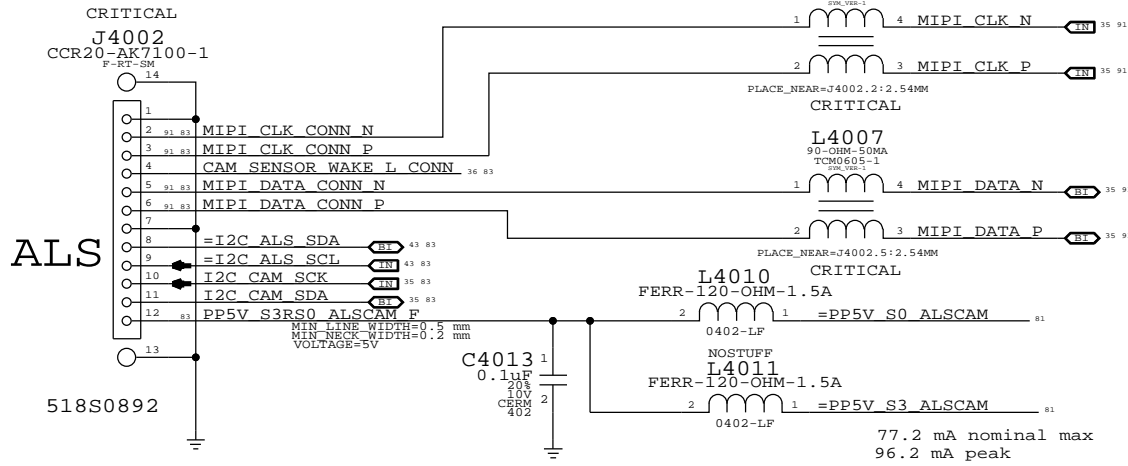


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		REVISION	6.0.0
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CAMERA SENSOR



remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

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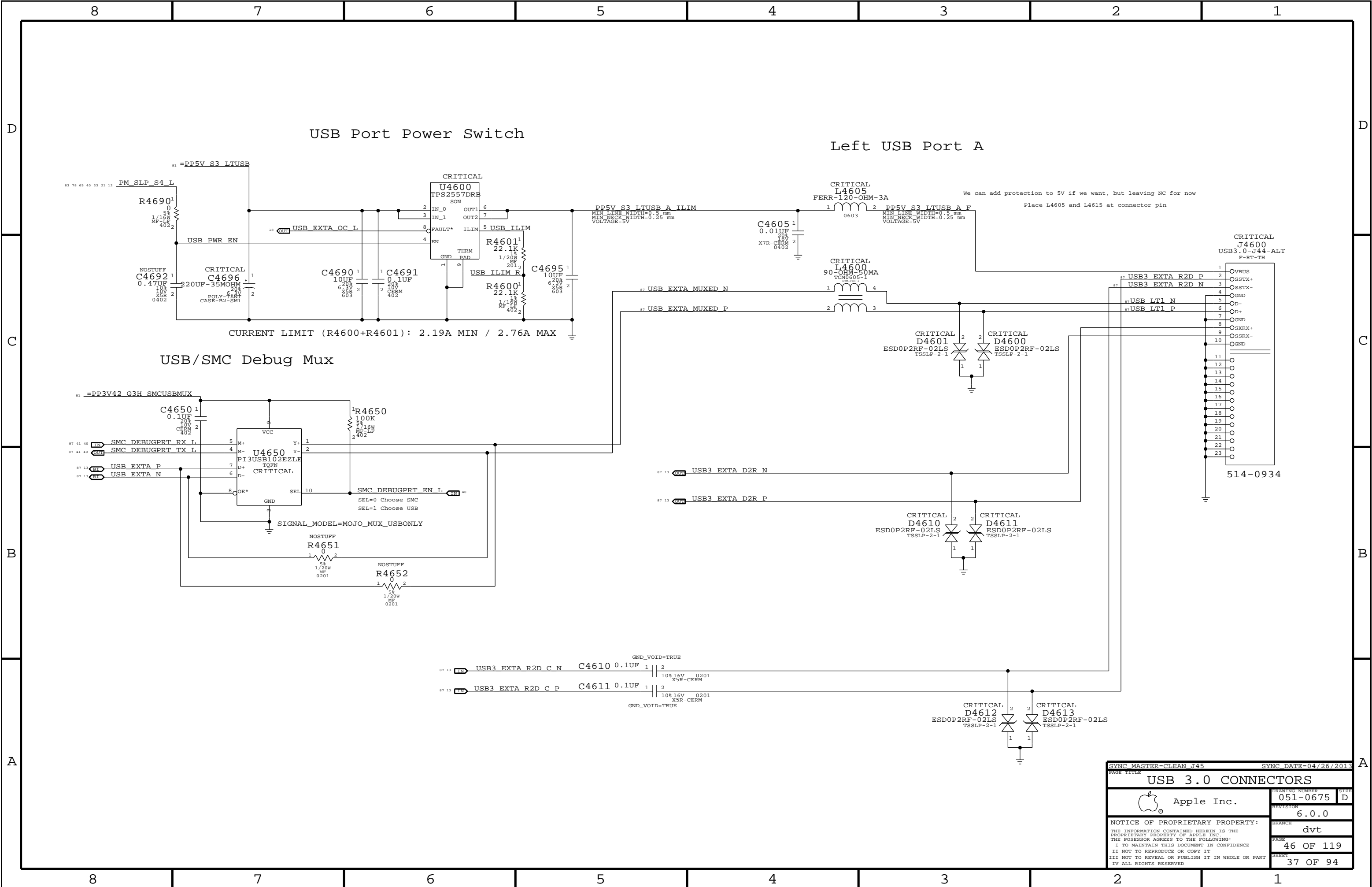
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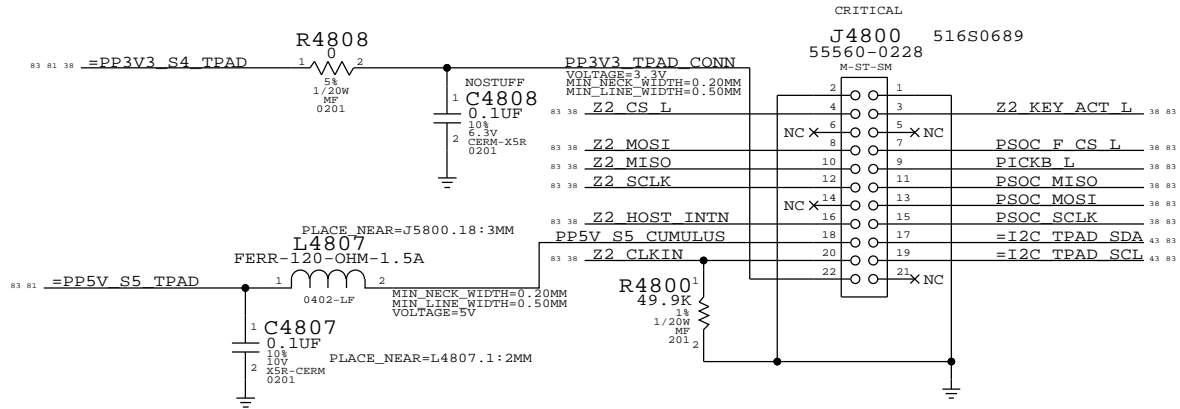
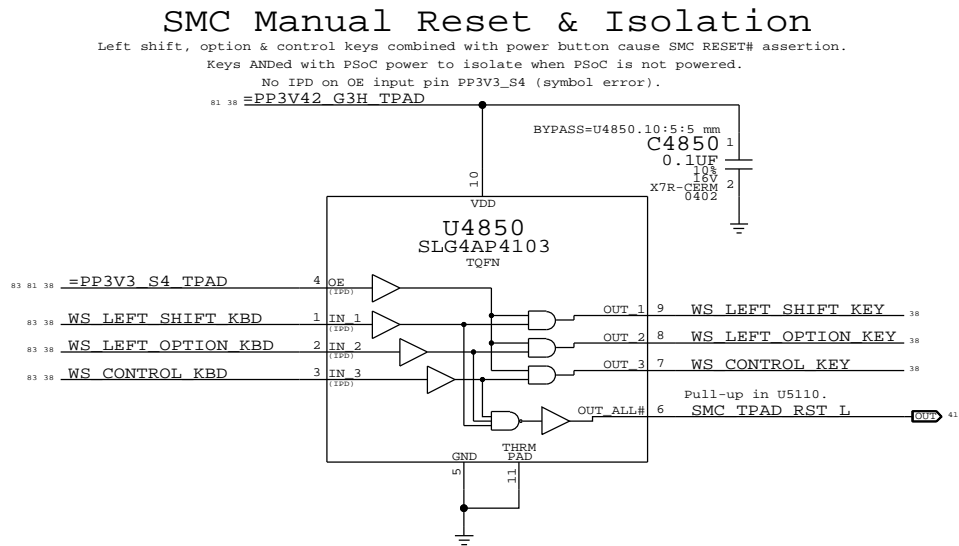
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SYNC DATE=04/26/2013



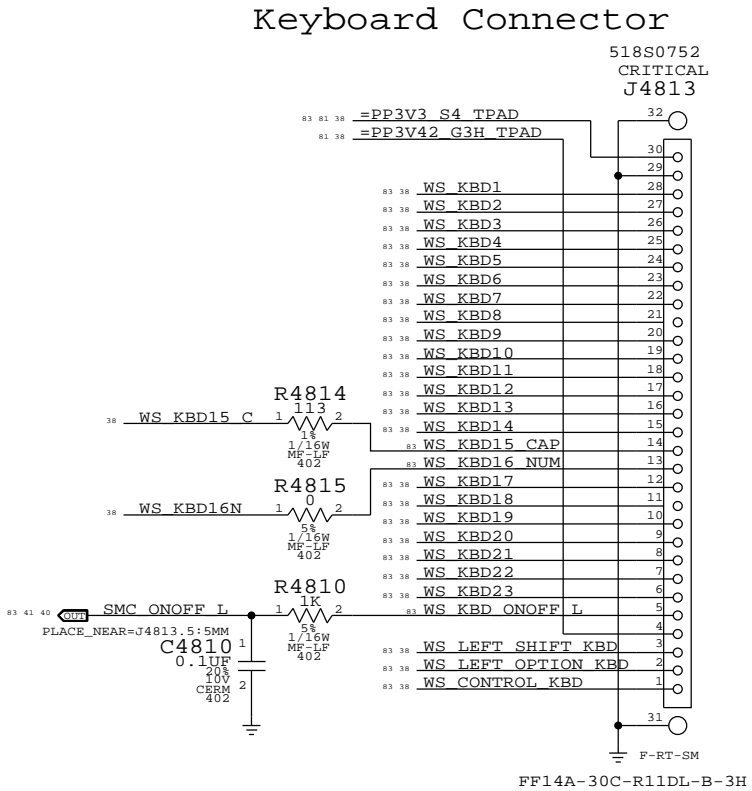
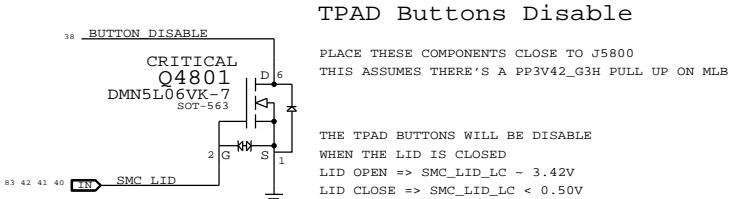
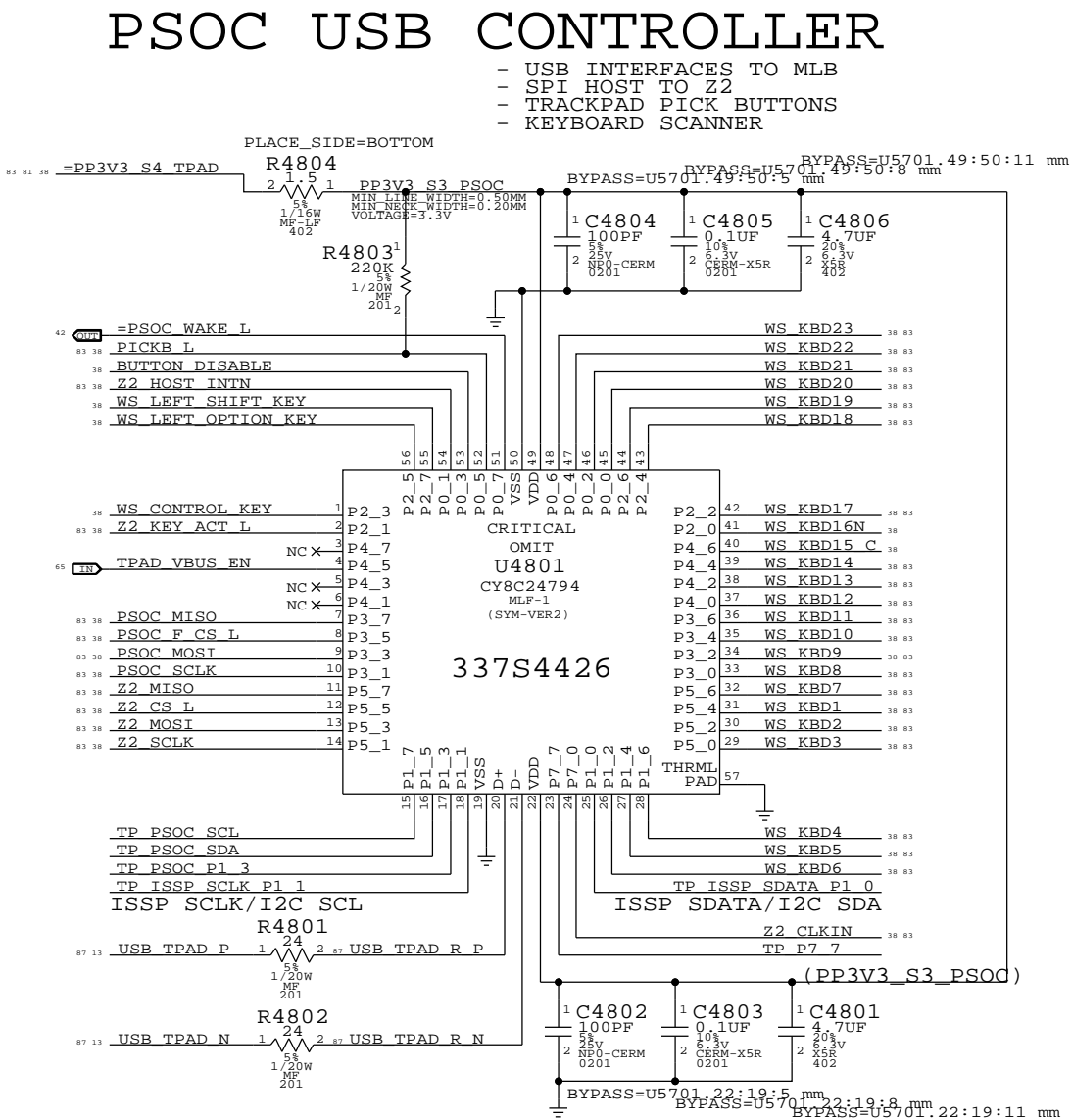
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IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA		2.55 KOHM	0.0255 V	0.255E-6 W
		80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM		0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM		0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM		0.012 V	96E-6 W
		14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM		0.0188 V	75.2E-6 W

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Keyboard Backlight Connector

516S0899  
CRITICAL  
J4915  
AA07A-S010-VA1  
P-ST-SM

83 62 KBDBKLT\_RETURN1

83 62 KBDBKLT\_RETURN2

83 62 PPVOUT\_S0\_KBDBKLT

12  
11

2 1  
4 3  
6 5  
8 7  
10 9

NC X NC

13  
14

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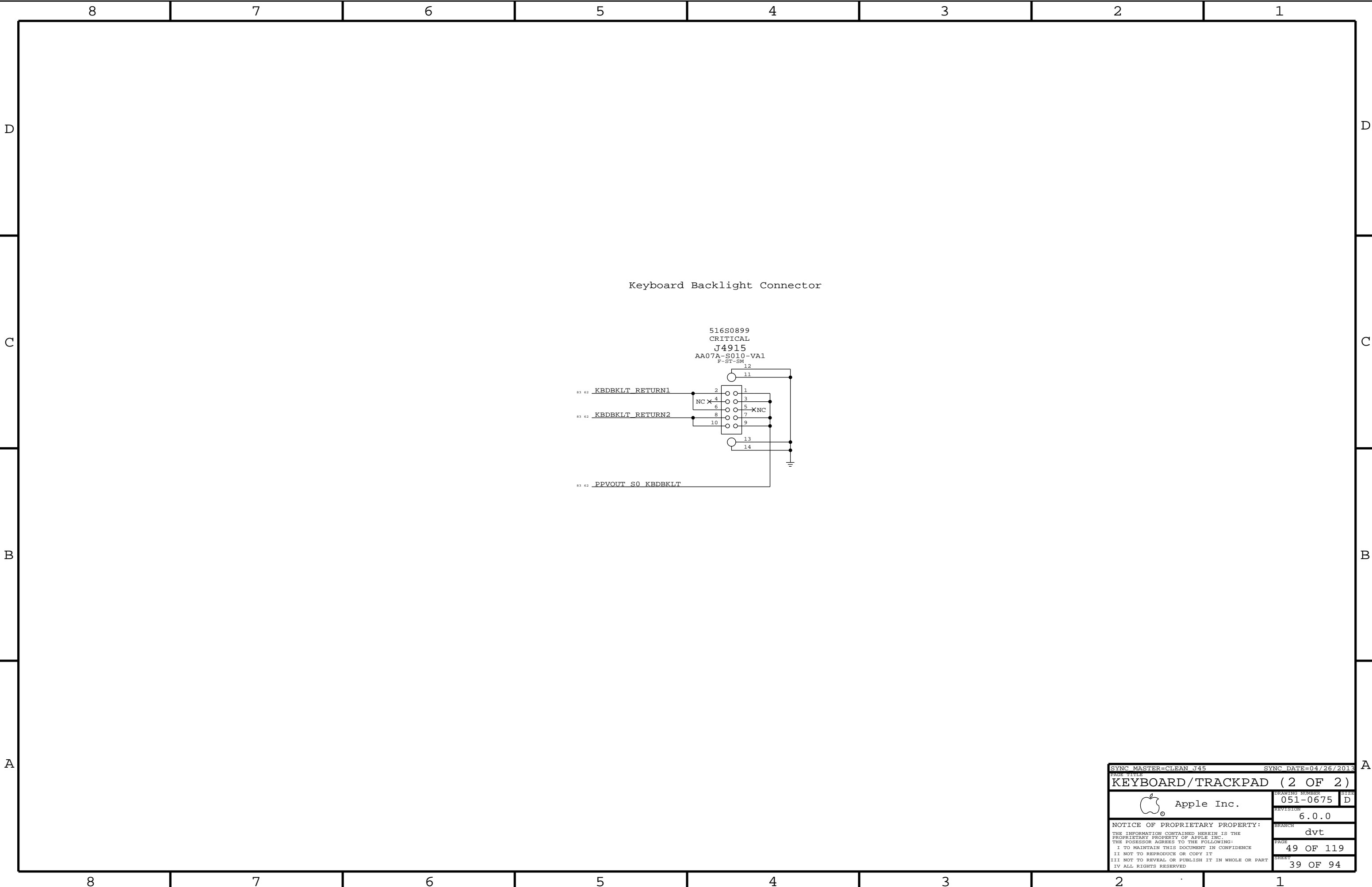
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8 7 6 5 4 3 2 1



8 7 6 5 4 3 2 1

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Keyboard Backlight Connector

516S0899  
CRITICAL  
J4915  
AA07A-S010-VA1  
P-ST-SM

83 62 KBDBKLT\_RETURN1

83 62 KBDBKLT\_RETURN2

83 62 PPVOUT\_S0\_KBDBKLT

12  
11

2 1  
4 3  
6 5  
8 7  
10 9

NC X NC

13  
14

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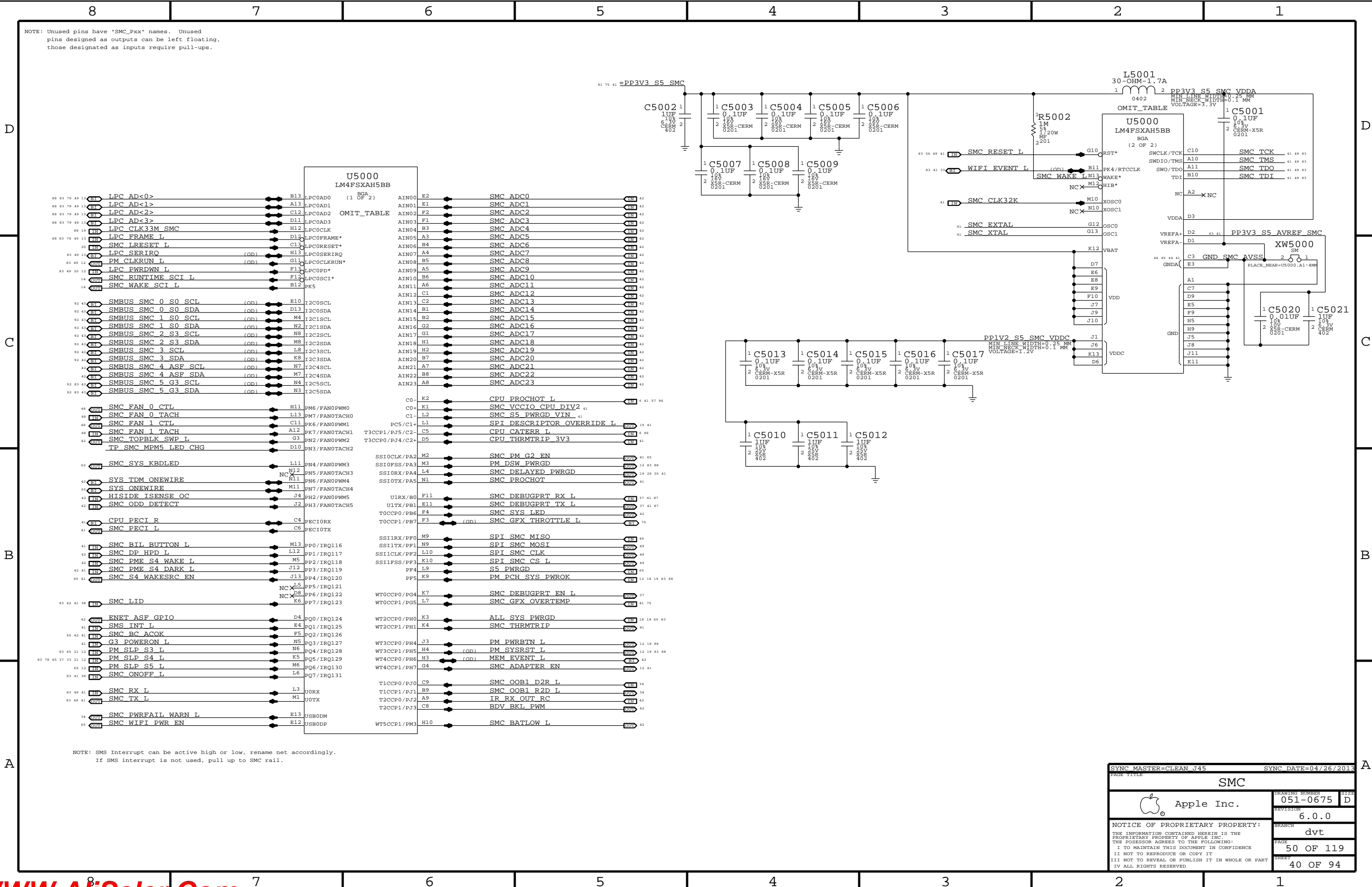
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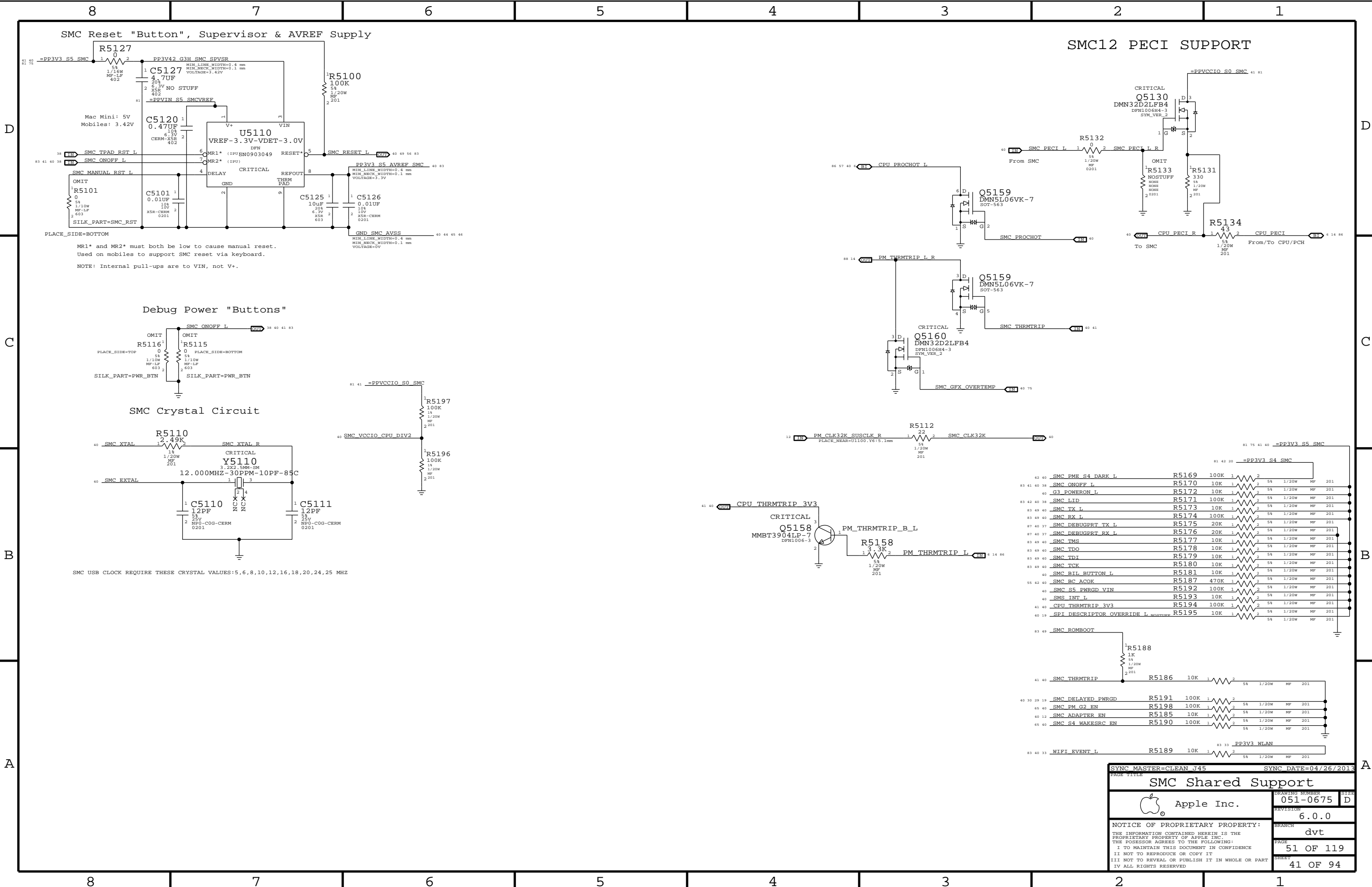
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SMC Shared Support

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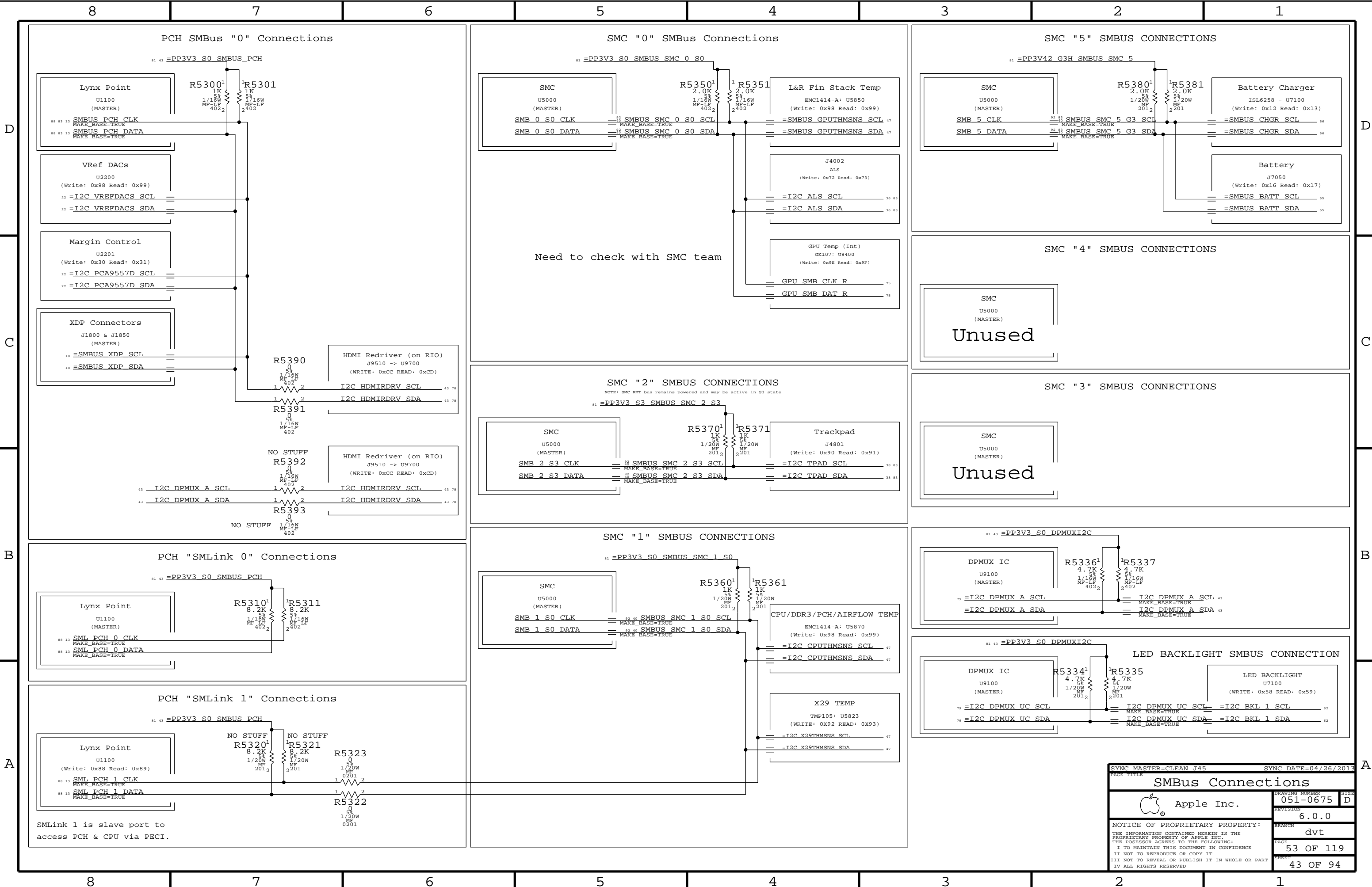
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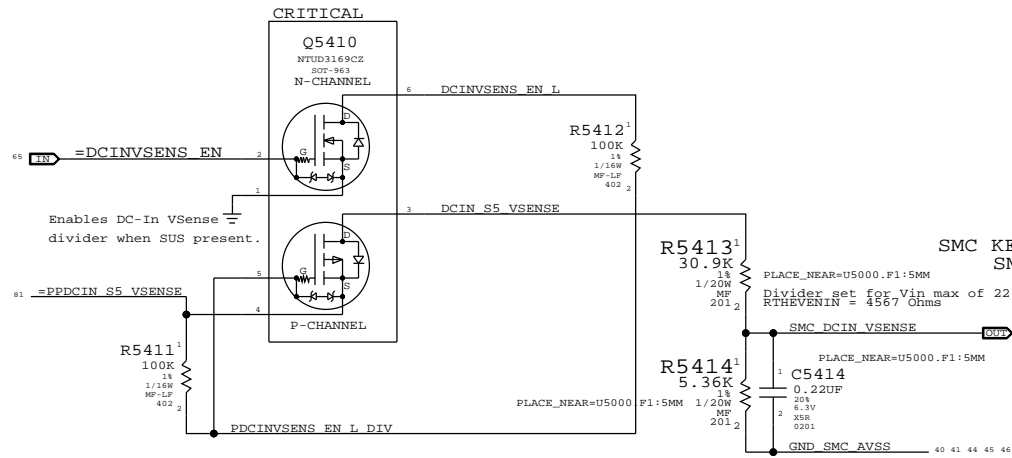
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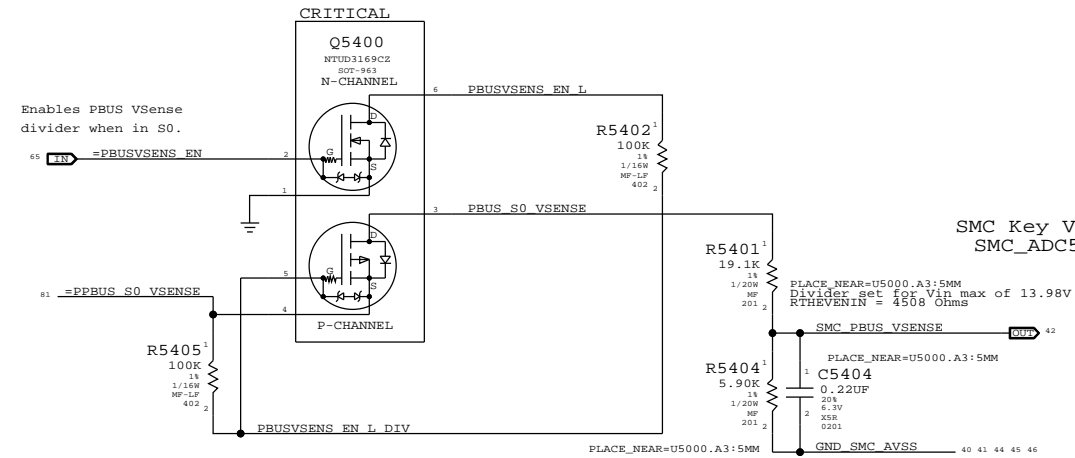




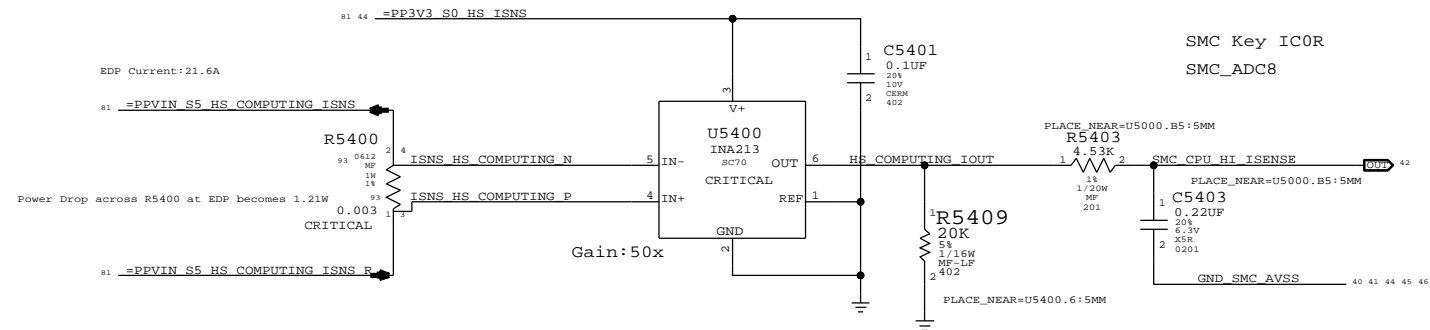
# DC-In Voltage Sense Enable & Filter



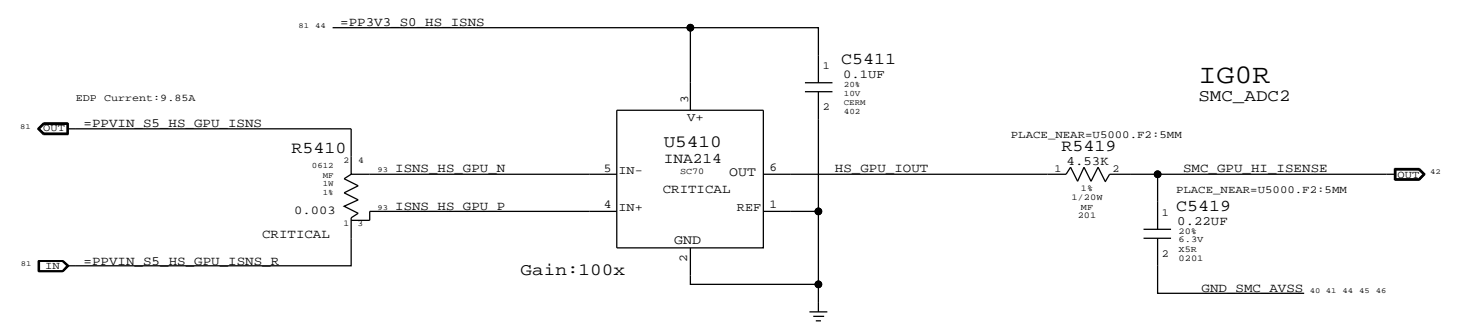
# PBUS Voltage Sense Enable & Filter



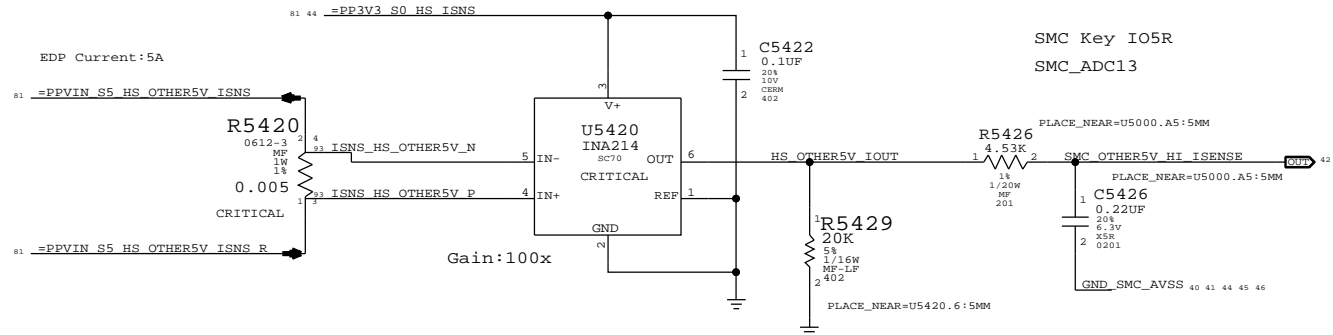
# COMPUTING High Side Current Sense / Filter



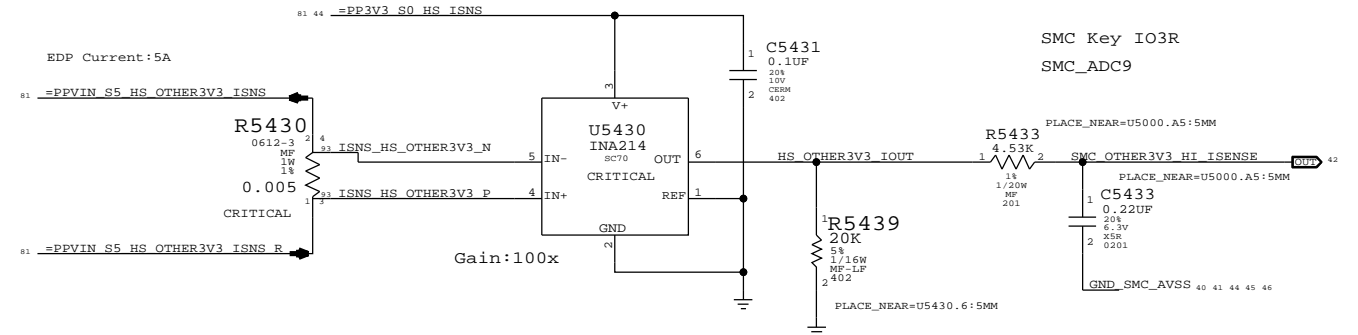
# GRAPHICS High Side Current Sense / Filter



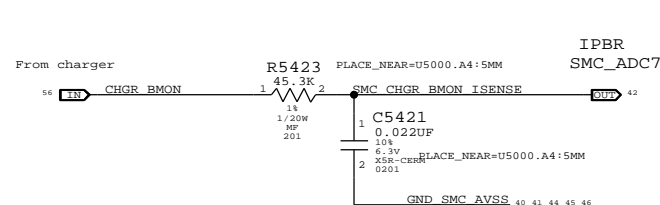
# OTHERS (5V) High Side Current Sense / Filter



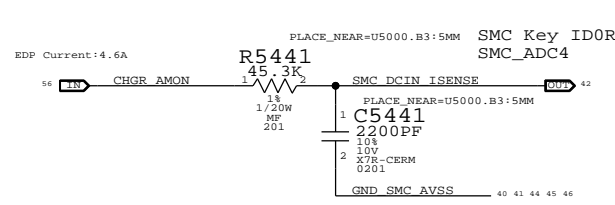
# OTHERS (3.3V) High Side Current Sense / Filter



# CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



# DC-IN (AMON) Current Sense Filter



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PAGE TITLE		High Side Voltage and Current Sensing	
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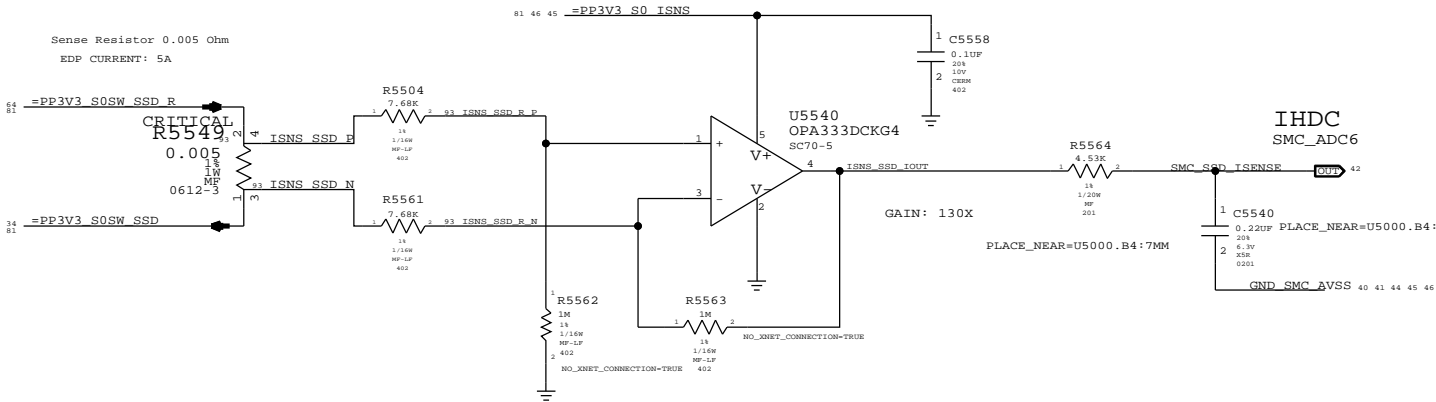
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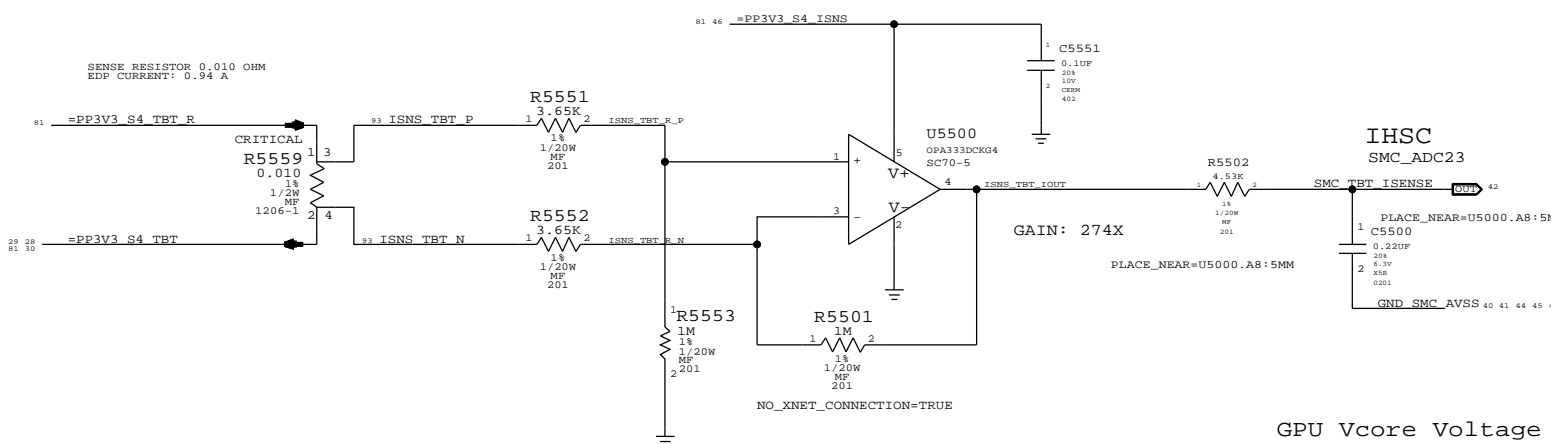
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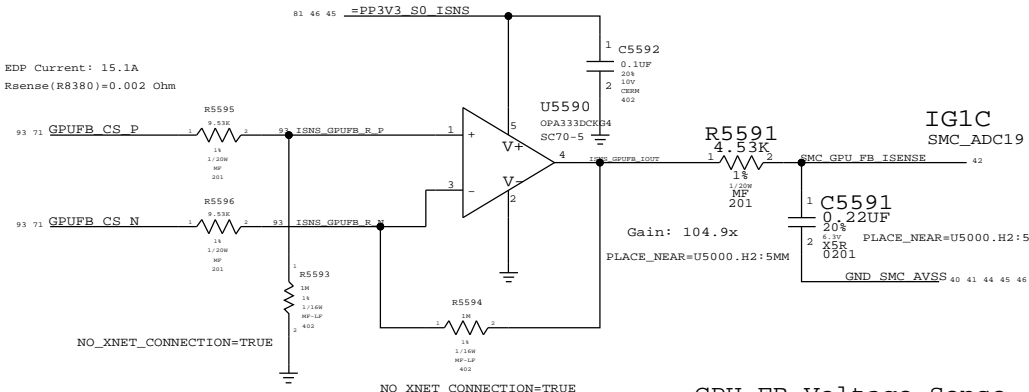
SSD CURRENT SENSE



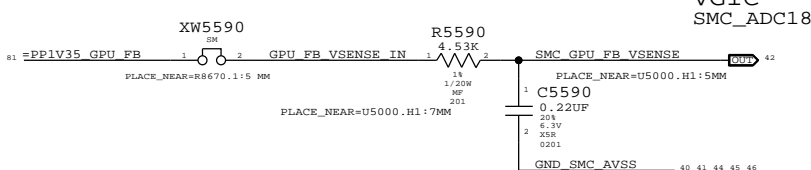
TBT Router CURRENT SENSE



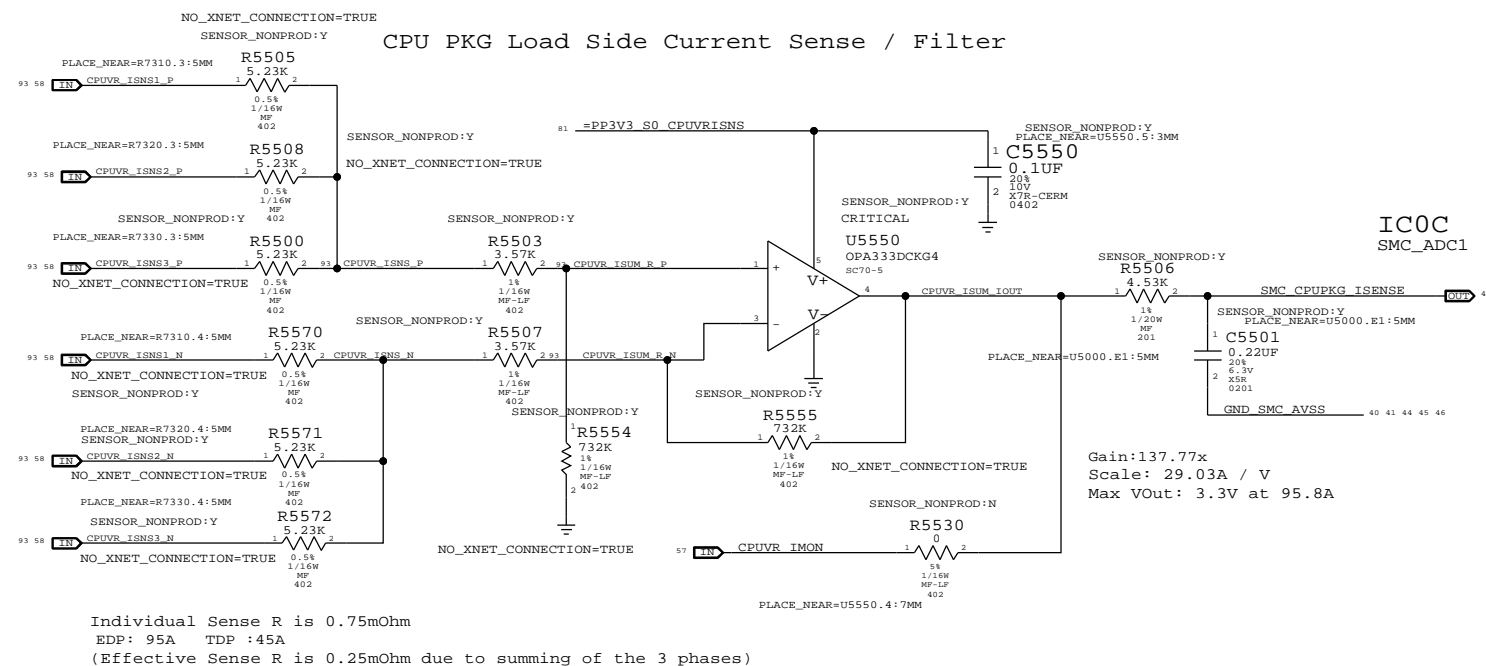
GPU FB (1.35V/1.5V) CURRENT SENSE



GPU FB Voltage Sense / Filter

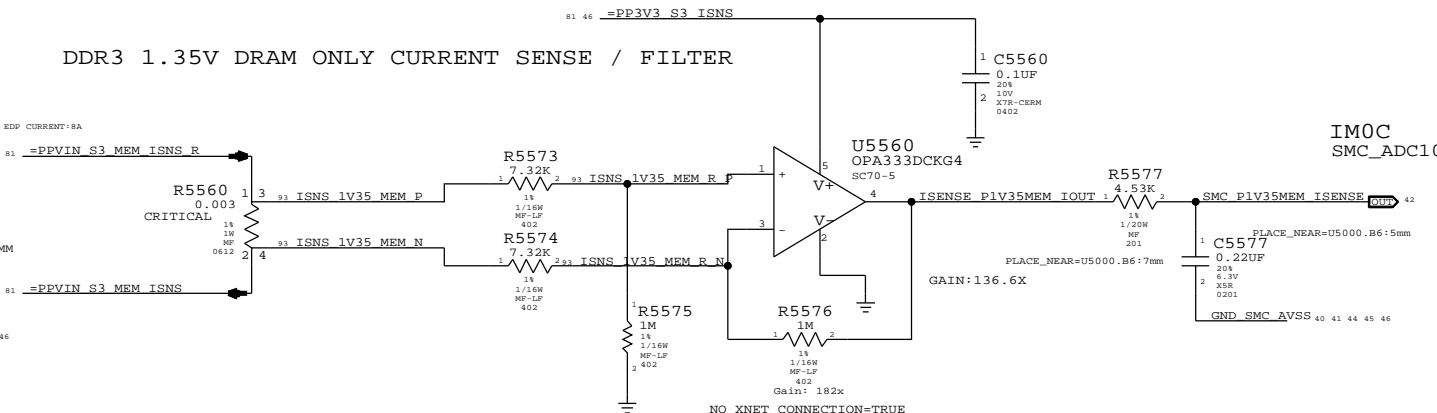


CPU PKG Load Side Current Sense / Filter

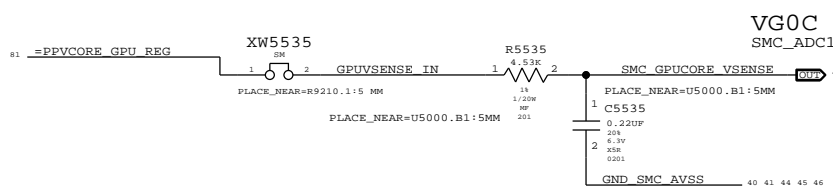


Individual Sense R is 0.75mOhm  
EDP: 95A TDP :45A  
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

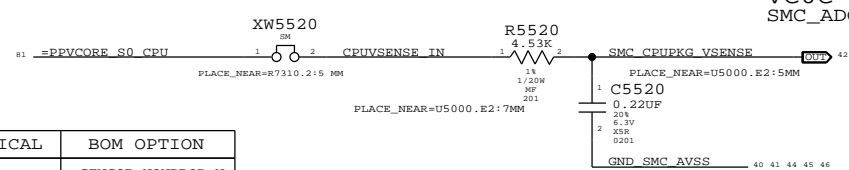
DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



GPU Vcore Voltage Sense / Filter



CPU Vcore Voltage Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MTL FILM,0,5,1/20W,0201,SMD,LF	R5506		SENSOR_NONPROD:N

removed LCD BKLIT Voltage Sensing

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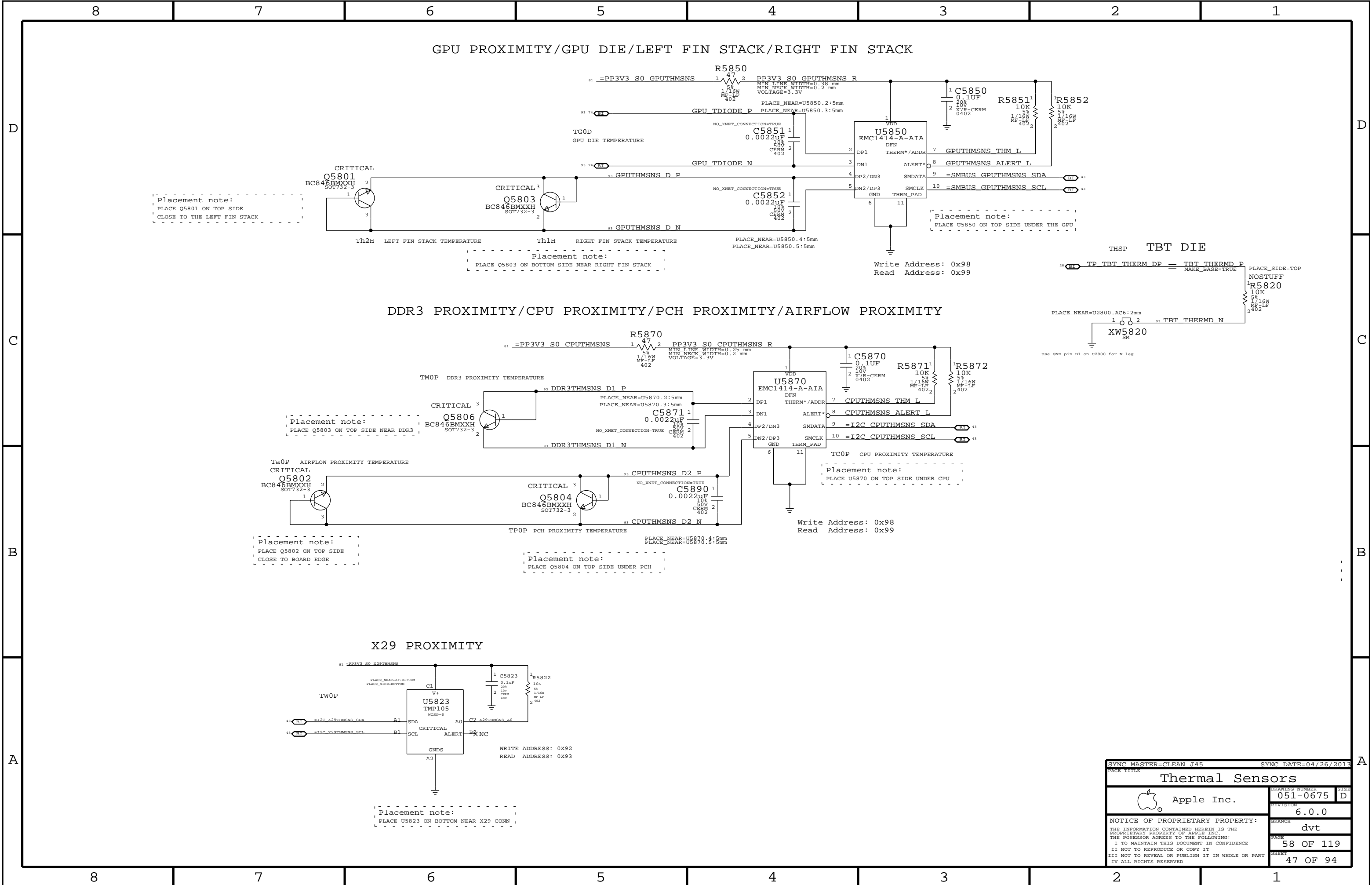
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
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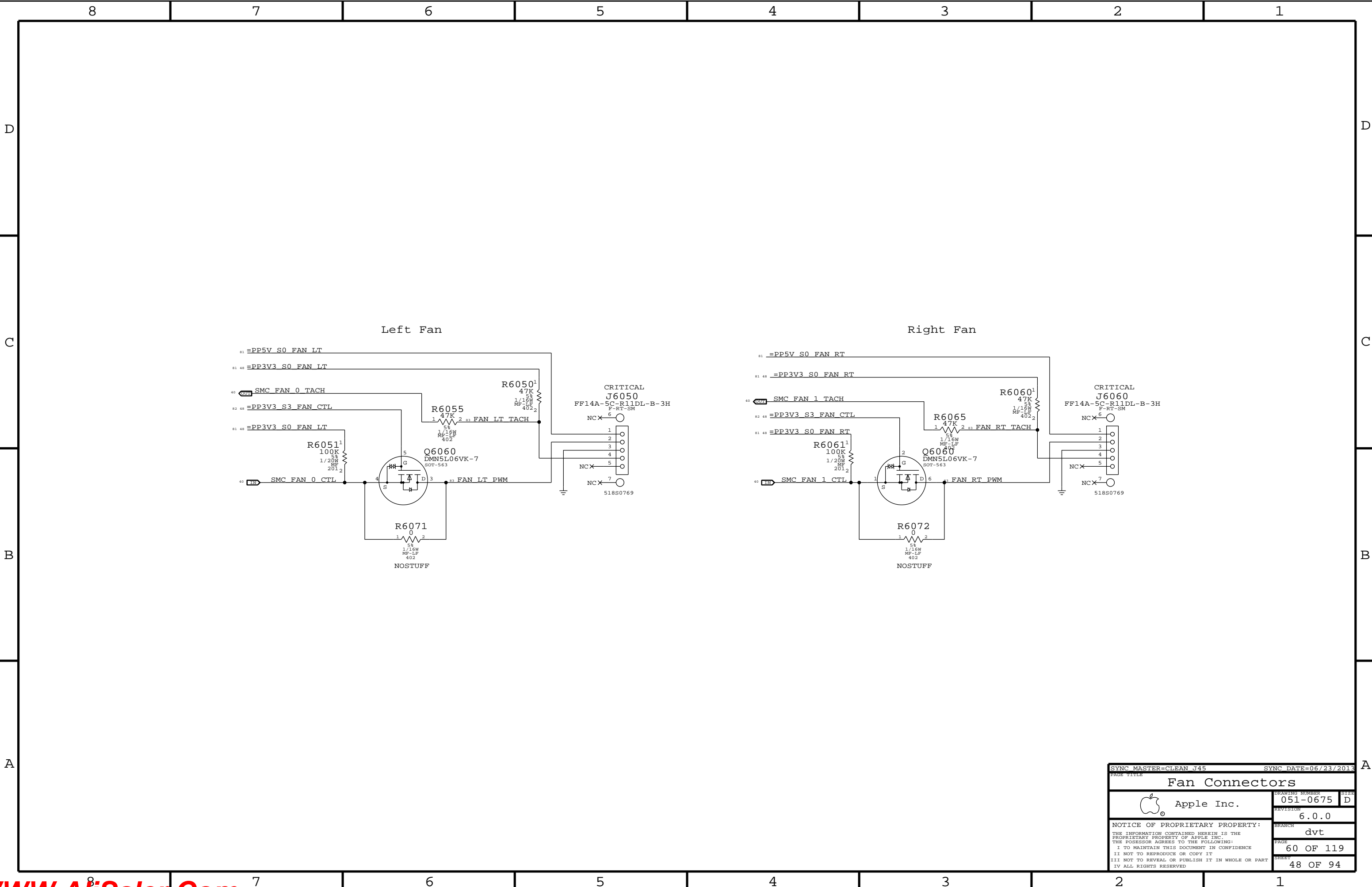
Load Side Voltage and Current Sensing








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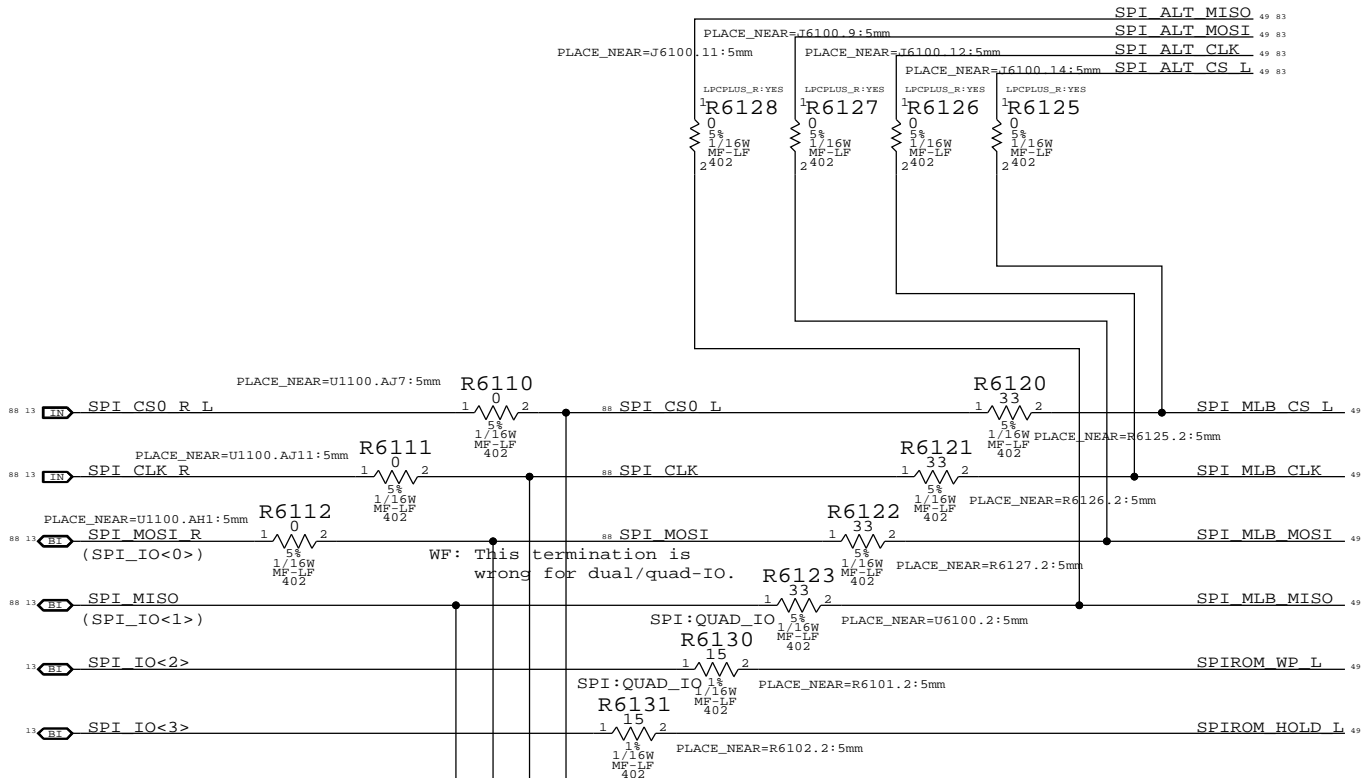
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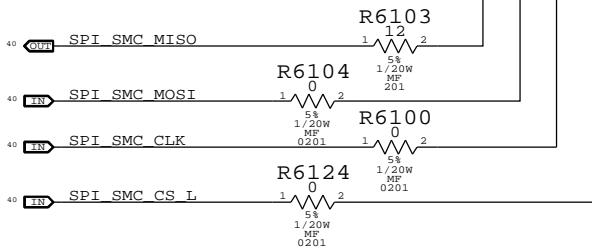
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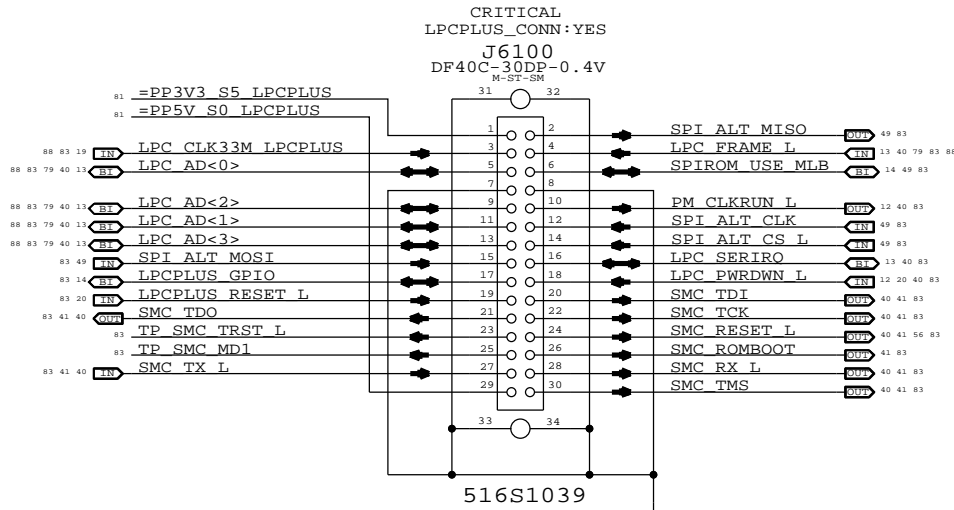
SPI Bus Series Termination



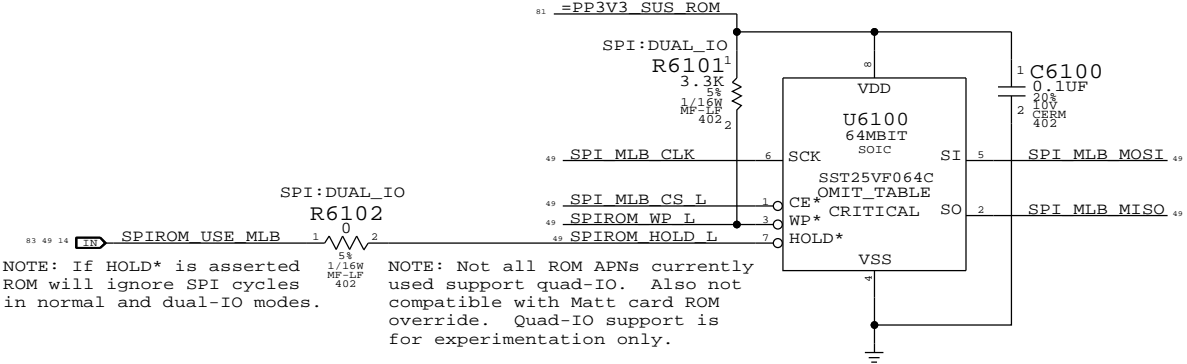
SMC12 SPI SUPPORT



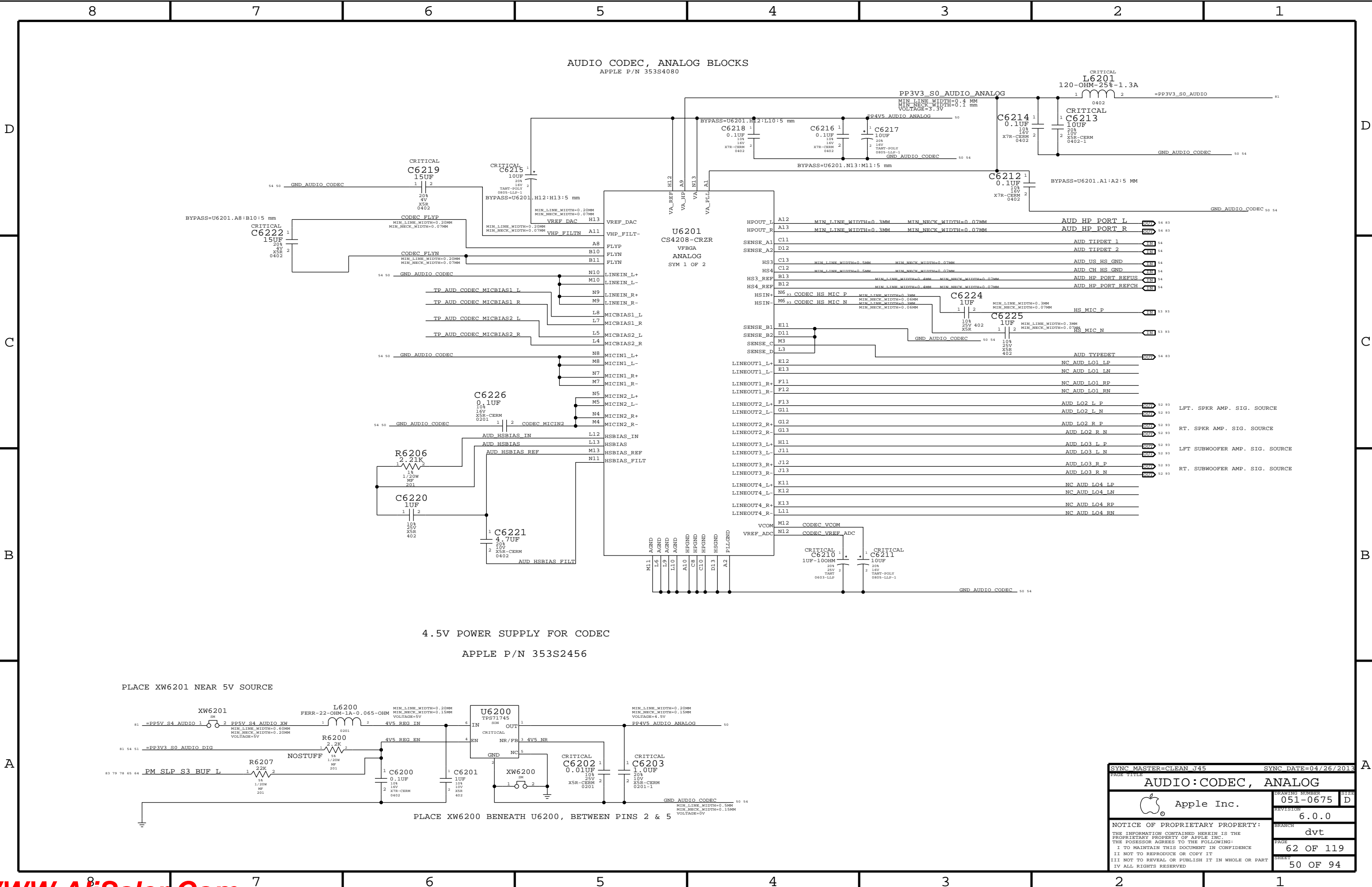
LPC+SPI Connector




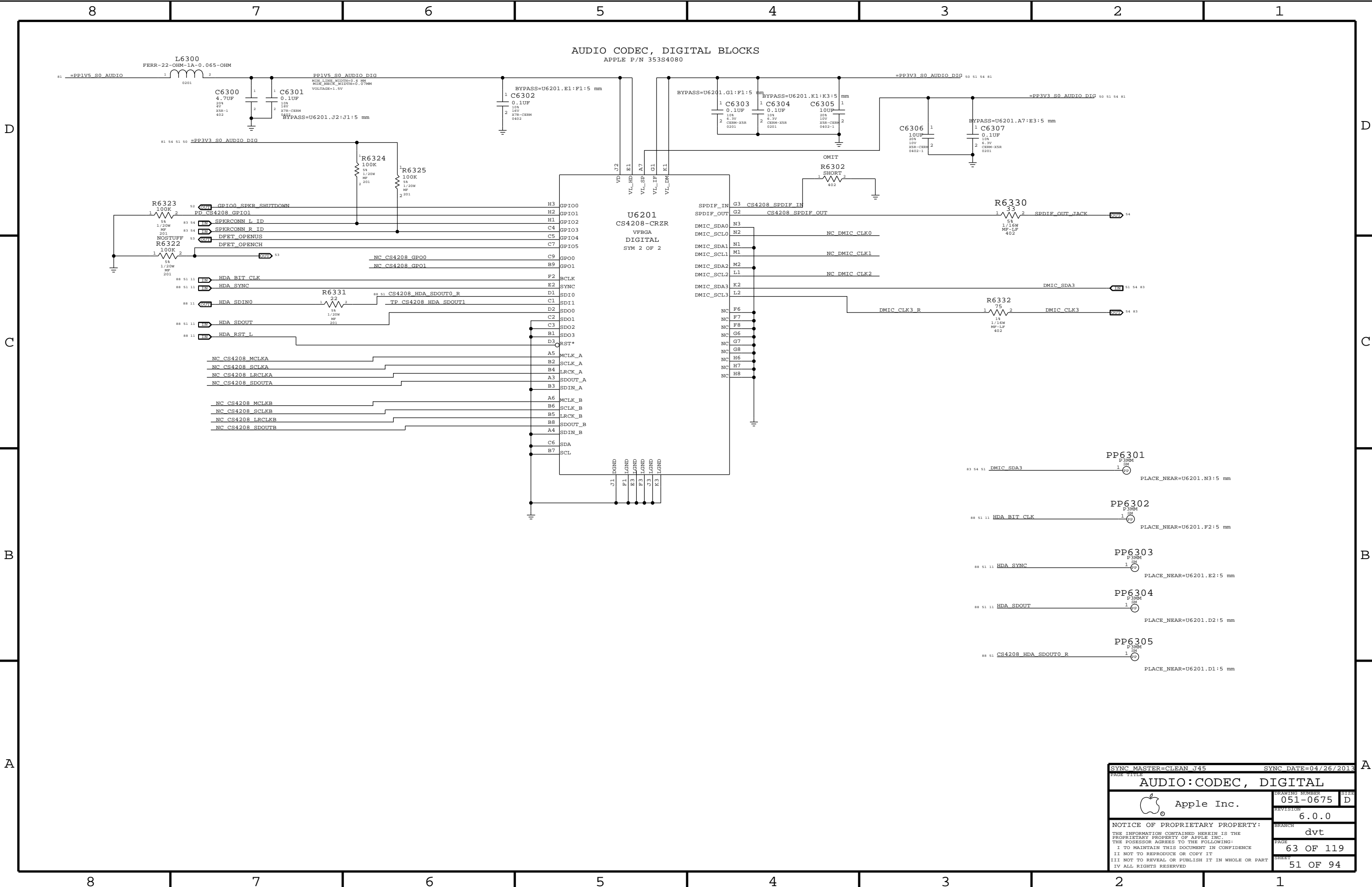
SPI ROM




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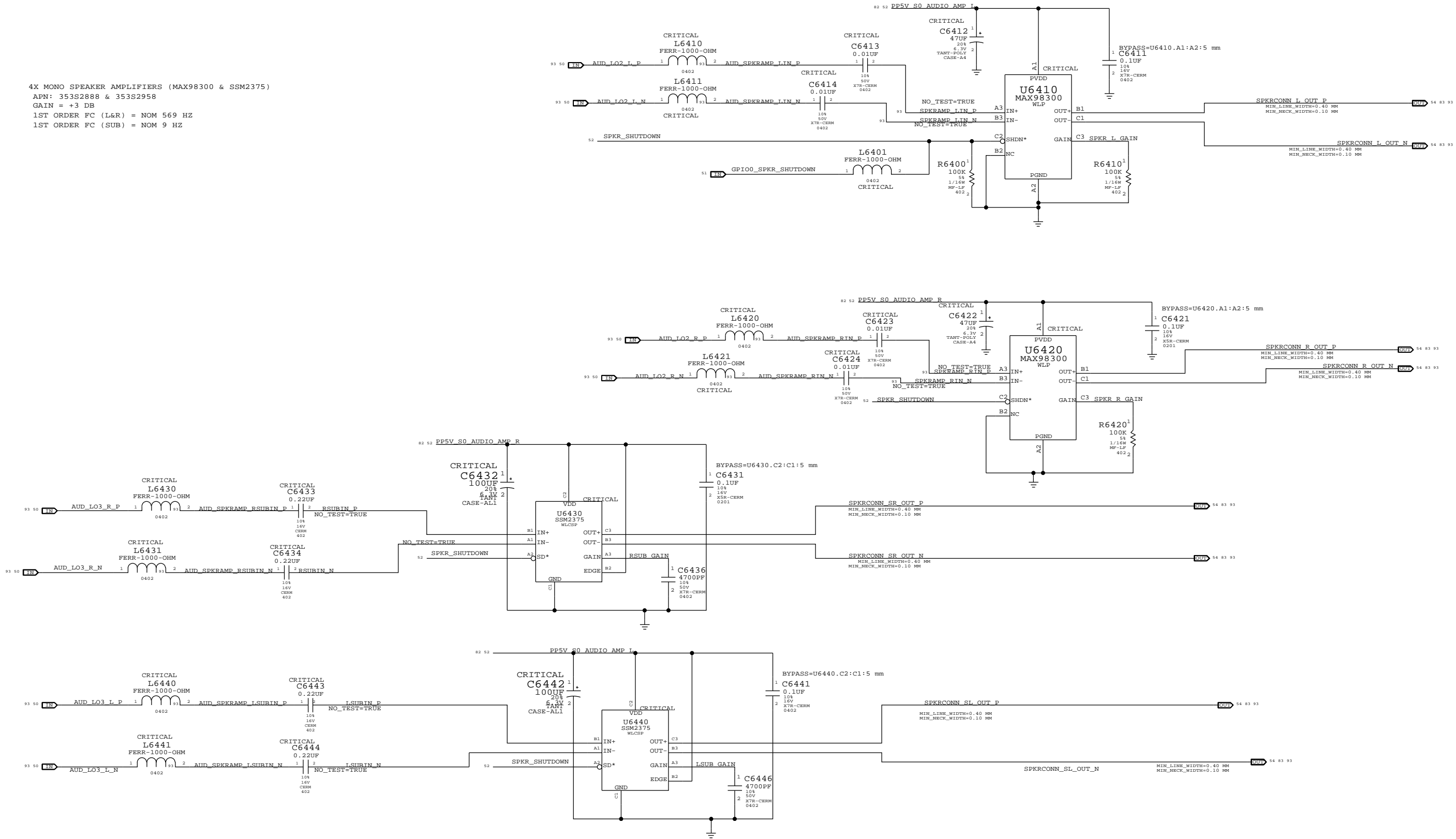



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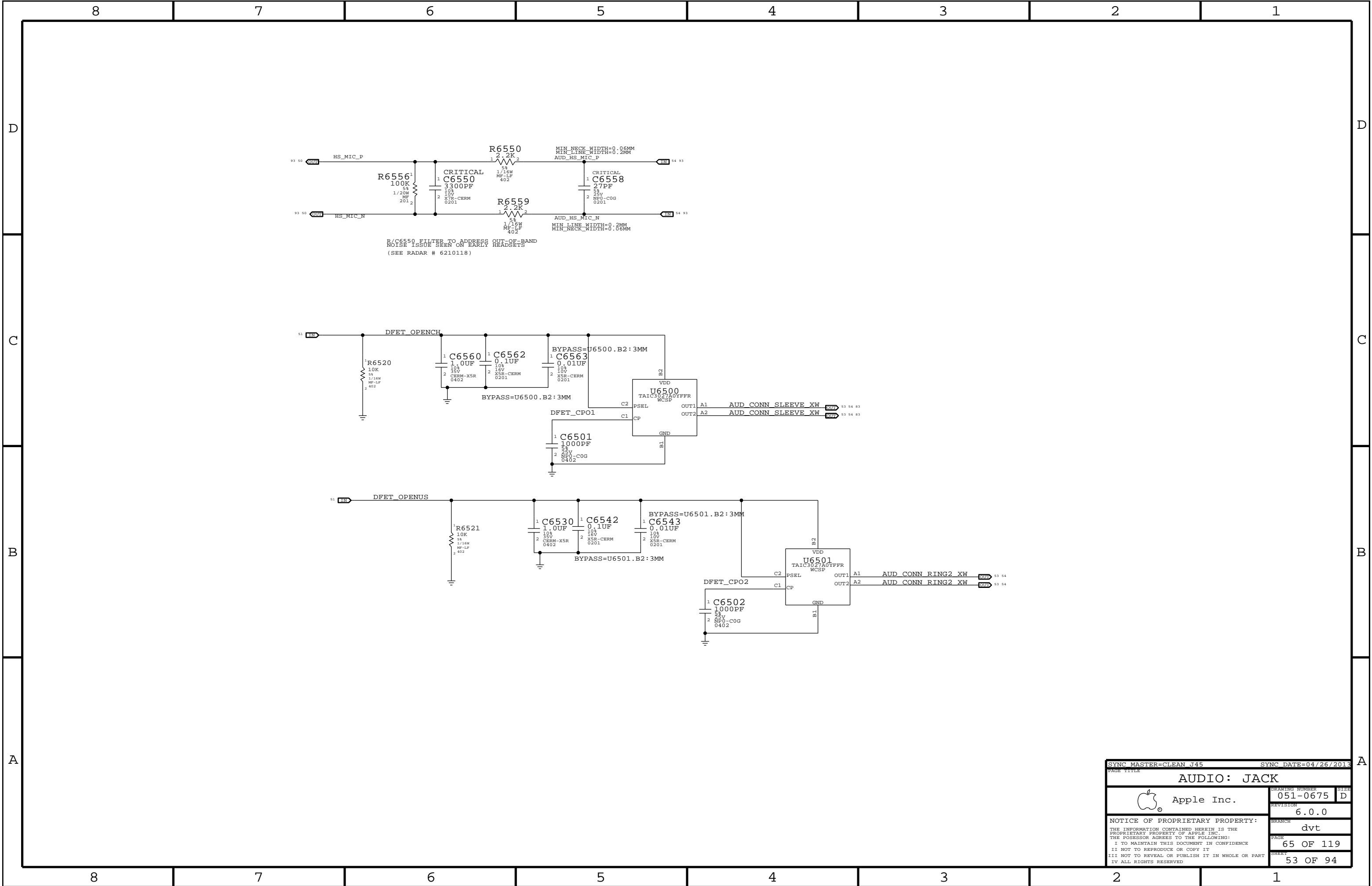
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	REVISION	6.0.0	
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4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)  
APN: 353S2888 & 353S2958  
GAIN = +3 DB  
1ST ORDER FC (L&R) = NOM 569 HZ  
1ST ORDER FC (SUB) = NOM 9 HZ



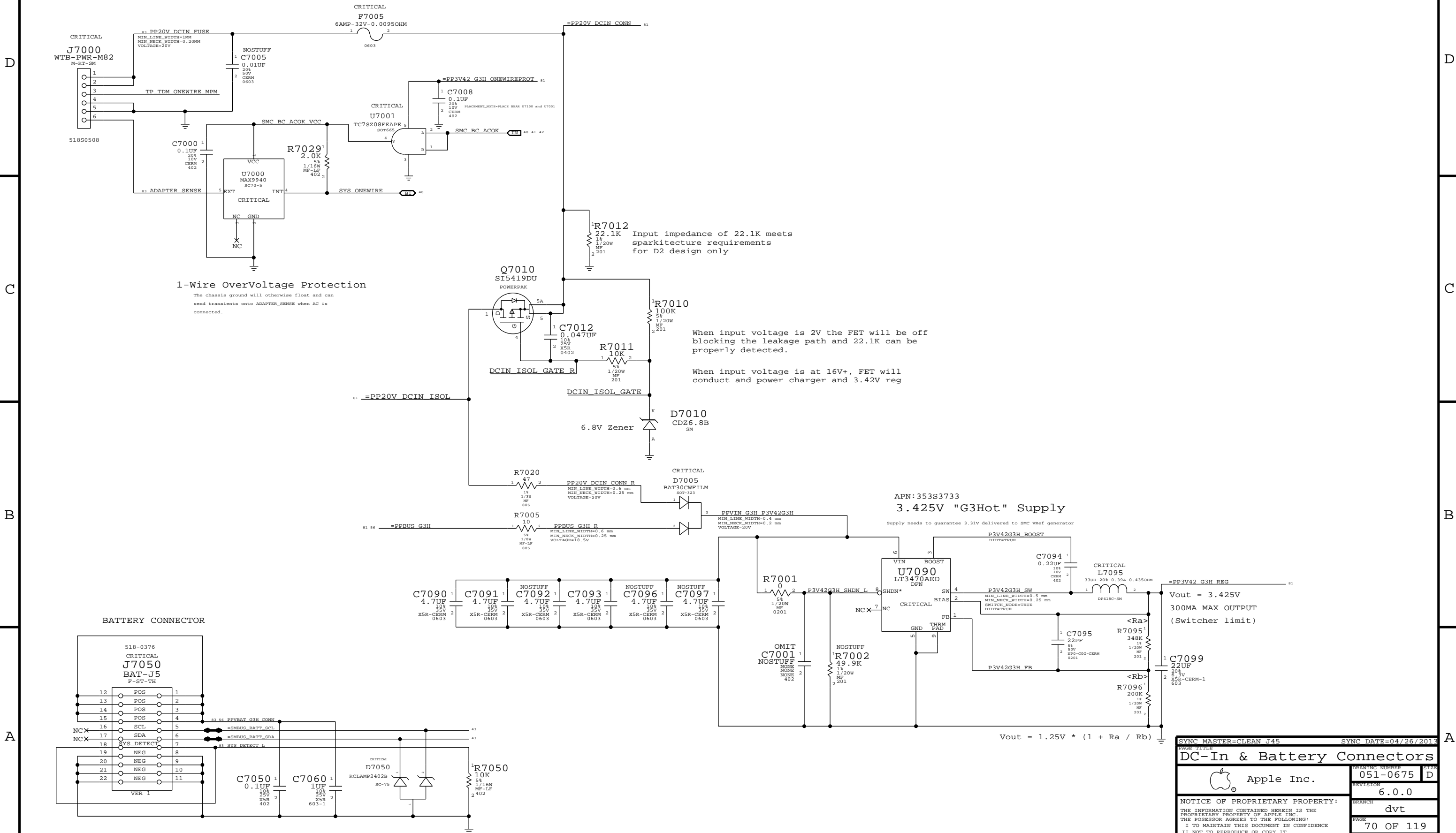
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		SHEET	52 OF 94



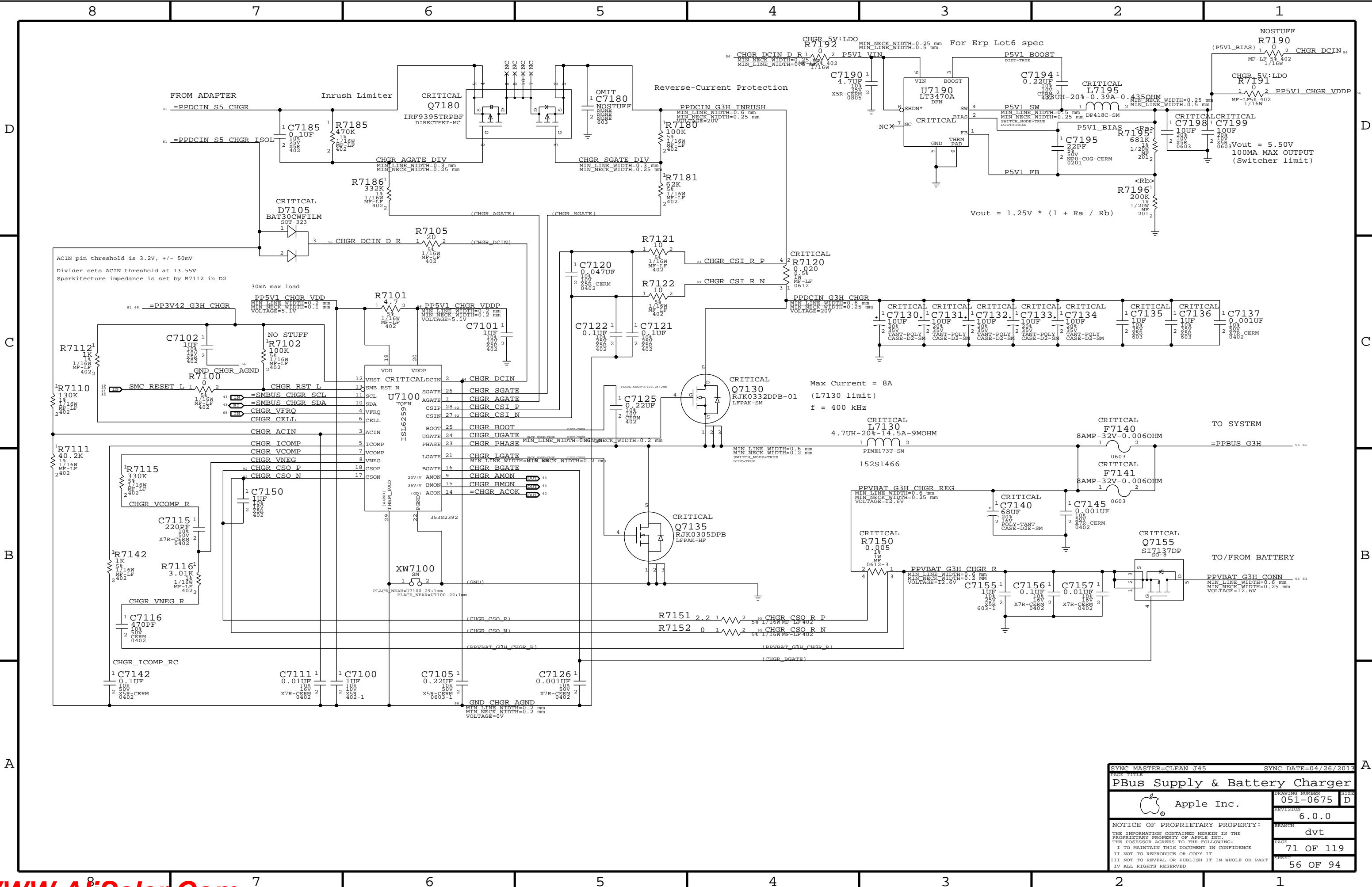





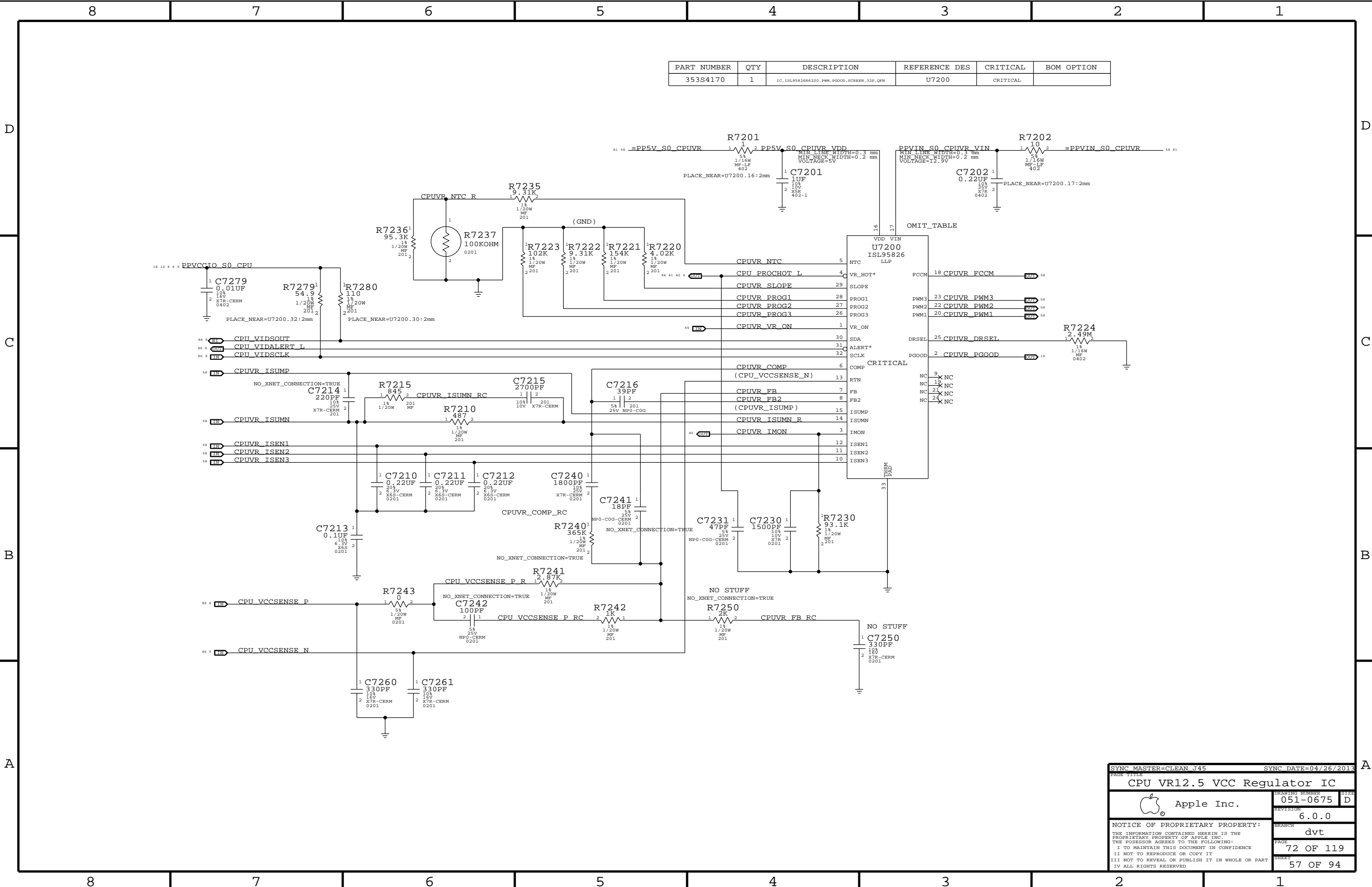
MagSafe DC Power Jack



PAGE TITLE		SYNC DATE=04/26/2013	
DC-In & Battery Connectors		DRAWING NUMBER	051-0675
Apple Inc.		REVISION	6.0.0
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SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	051-0675
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PWM, PGOOD, SCREEN, 32P, QFN	U7200	CRITICAL	

PAGE TITLE		PAGE NUMBER	
CPU VR12.5 VCC Regulator IC		051-0675	
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## D

B



1V05 S0 REGULATOR

Vout = 0.5V \* (1 + Ra / Rb)

Vout = 1.05V  
12A MAX OUTPUT  
f = 300 kHz

OCP = R7641 x 8.5uA / R7640  
OCP = 14.4A

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
1V05V POWER SUPPLY			
DRAWING NUMBER		SIZE	
051-0675		D	
REVISION		6.0.0	
BRANCH		dvt	
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SHEET		61 OF 94	

1V05 S0 REGULATOR

Vout = 0.5V \* (1 + Ra / Rb)

Vout = 1.05V  
12A MAX OUTPUT  
f = 300 kHz

OCP = R7641 x 8.5uA / R7640  
OCP = 14.4A

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
1V05V POWER SUPPLY			
DRAWING NUMBER		SIZE	
051-0675		D	
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1V05 S0 REGULATOR

Power aliases required by this page:

- =PPV1N_S0_LCDCKLIT	(9-12.6V LCD Backlight Input)
- =PPFV50_S0_BKLTCTRL	(5V Backlight Driver Input)
- =PPFV50_S0_KBDLED	(5V Keyboard Backlight Input)

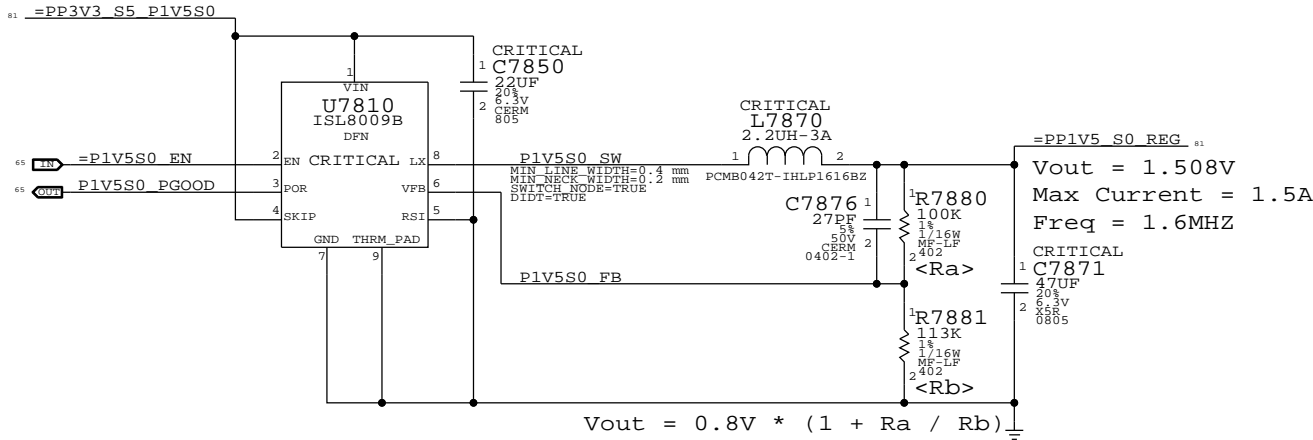
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BOM options provided by this page:

BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

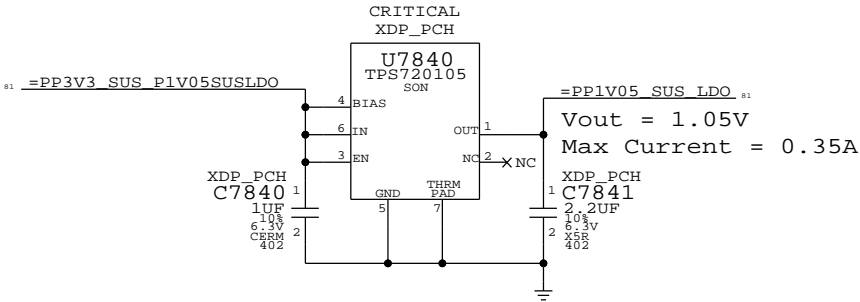
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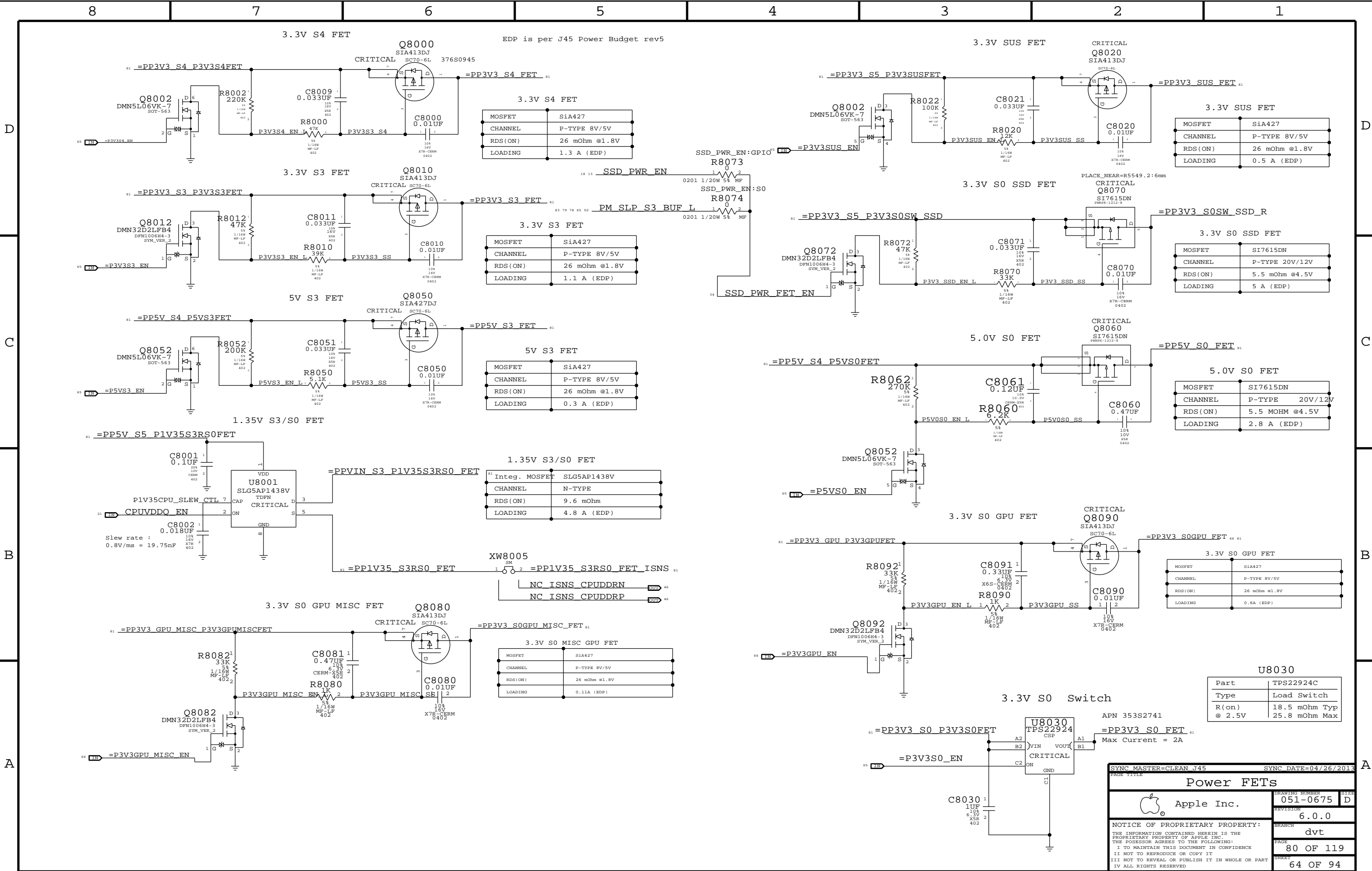
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.  
Pull-ups (3) must be 51 ohms to support XDP (not required in production).  
70mA is required to support pull-ups. Alternative is strong voltage  
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.





MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

MOSFET	Si7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

MOSFET	Si7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.6A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

SYNC MASTER=CLEAN J45

SYNC DATE=04/26/2013

Power FETs

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051-0675

SIZE

D

REVISION

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8	7	6	5	4	3	2	1
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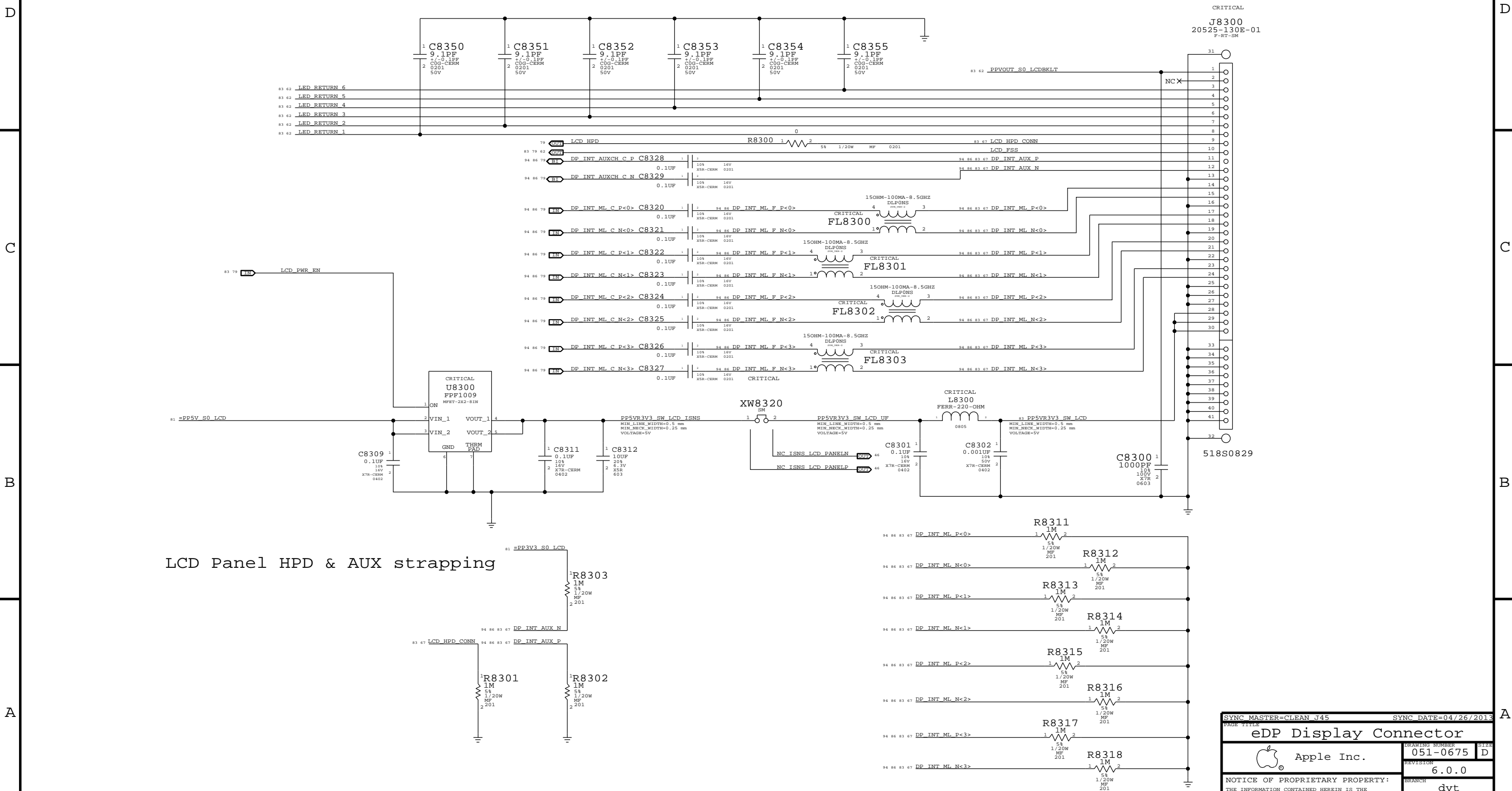
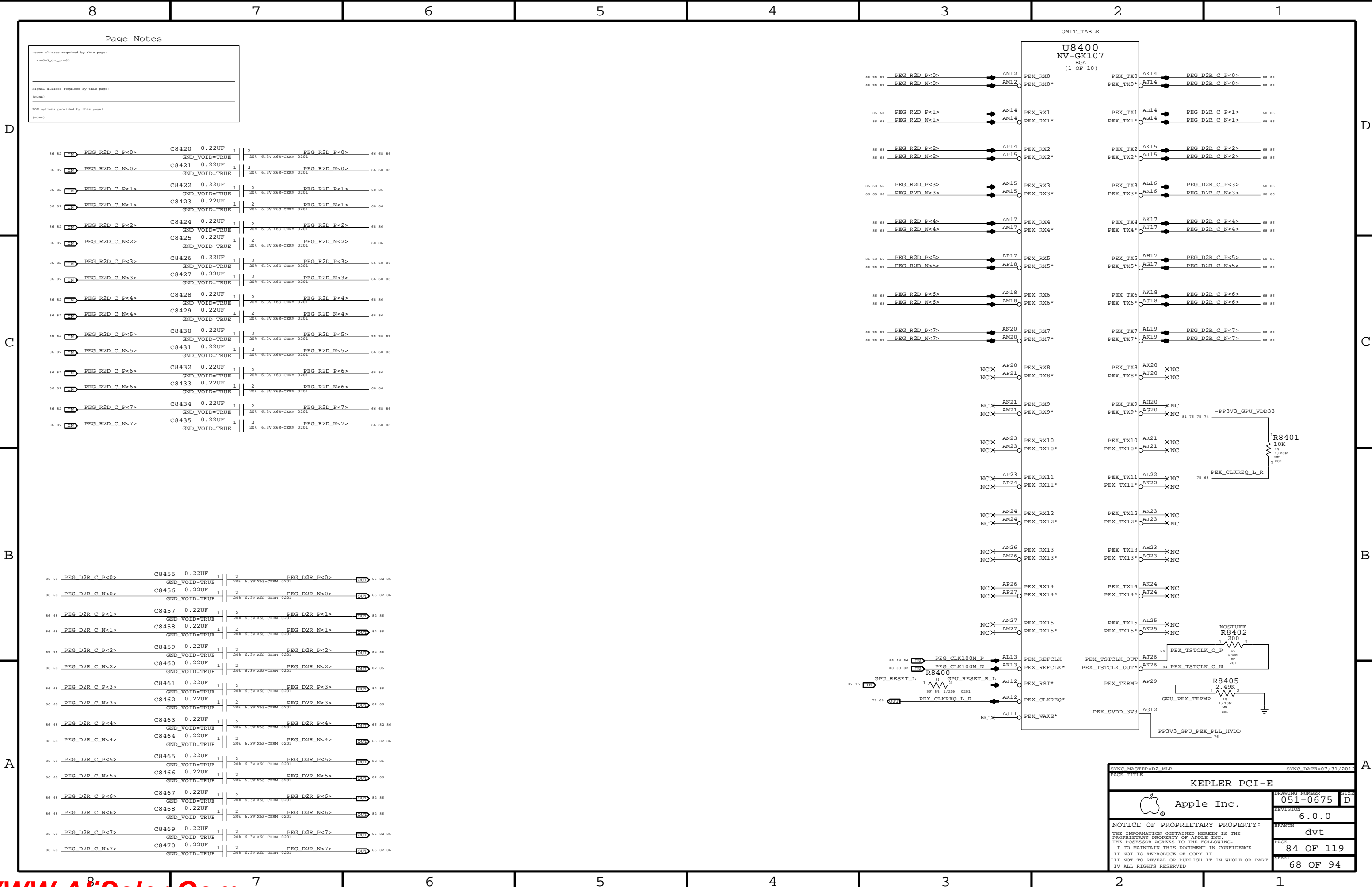


Diagram illustrating the eDP Display Connector circuit. The circuit shows two signal lines, DP\_INT\_ML\_P<3> and DP\_INT\_ML\_N<3>, each passing through a resistor network (R8317 and R8318) connected to a 1/20W 5% resistor network. The diagram also includes a title block with the following information:

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PAGE TITLE: eDP Display Connector			
DRAWING NUMBER: 051-0675		SIZE: D	
REVISION: 6.0.0		BRANCH: dvt	
PAGE: 83 OF 119		SHEET: 67 OF 94	

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Power aliases required by this page:  
--PP3V3\_GPU\_VDD33

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)


86 82	MIN	PEG R2D C P<0>	C8420 0.22UF	1	2	PEG R2D P<0>	68 68 86
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86 82	MIN	PEG R2D C N<0>	C8421 0.22UF	1	2	PEG R2D N<0>	68 68 86
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86 82	MIN	PEG R2D C P<1>	C8422 0.22UF	1	2	PEG R2D P<1>	68 86
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86 82	MIN	PEG R2D C N<1>	C8423 0.22UF	1	2	PEG R2D N<1>	68 86
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86 82	MIN	PEG R2D C P<4>	C8428 0.22UF	1	2	PEG R2D P<4>	68 86
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86 68	PEG D2R C N<5>	C8466 0.22UF	1	2	PEG D2R N<5>	82 86
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		GND_VOID=TRUE			204 6.3V X6S-CERN 0201	

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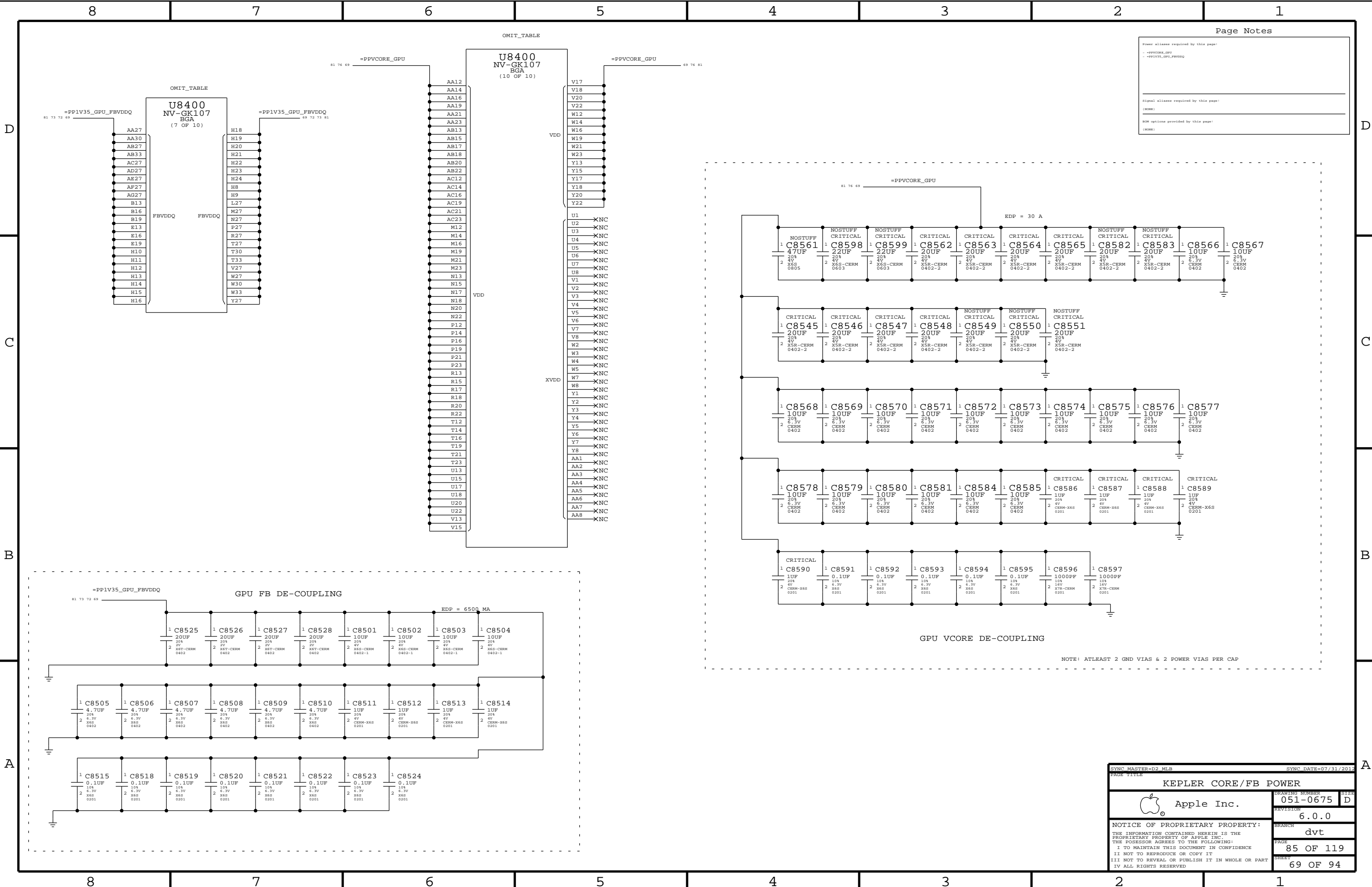
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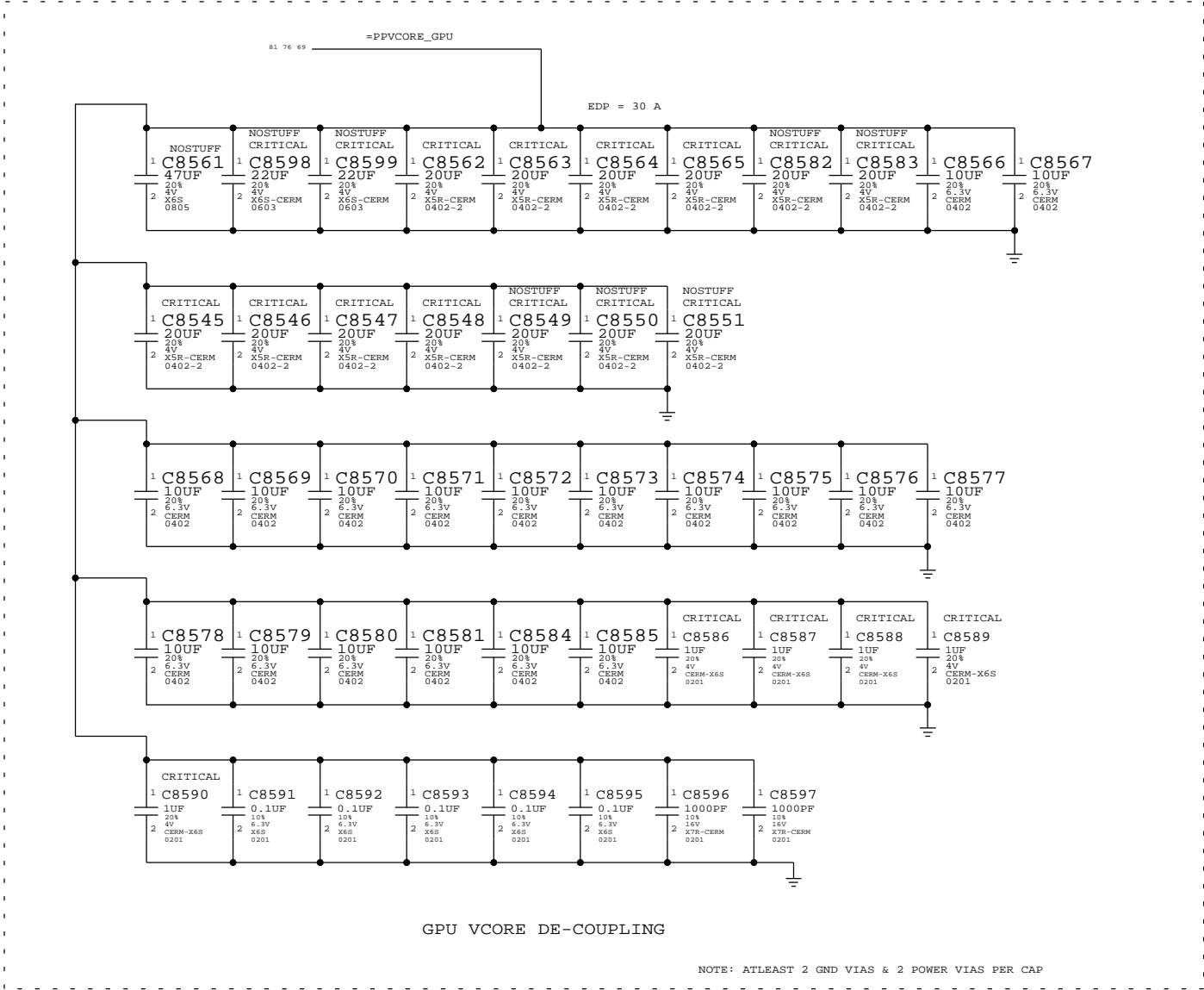
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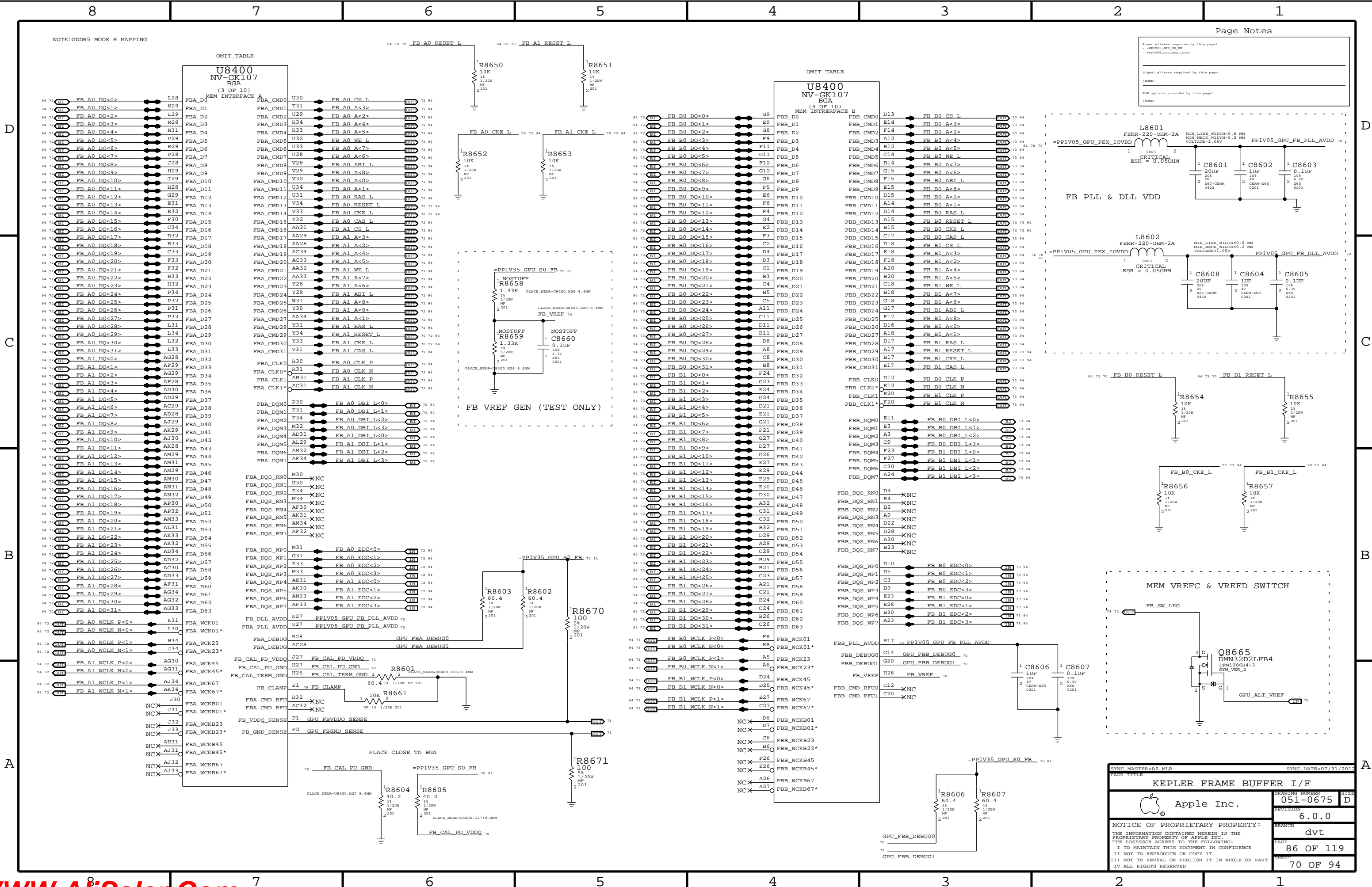
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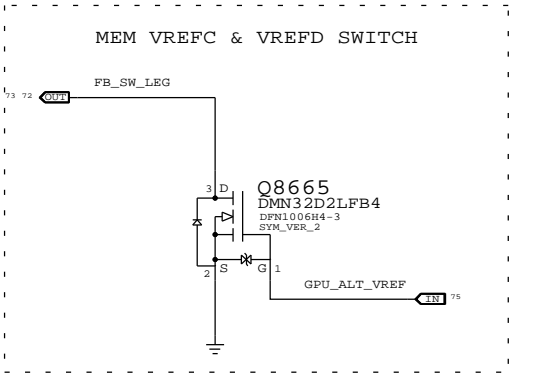
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- PPIV05\_GPU\_PEX\_IOVDD

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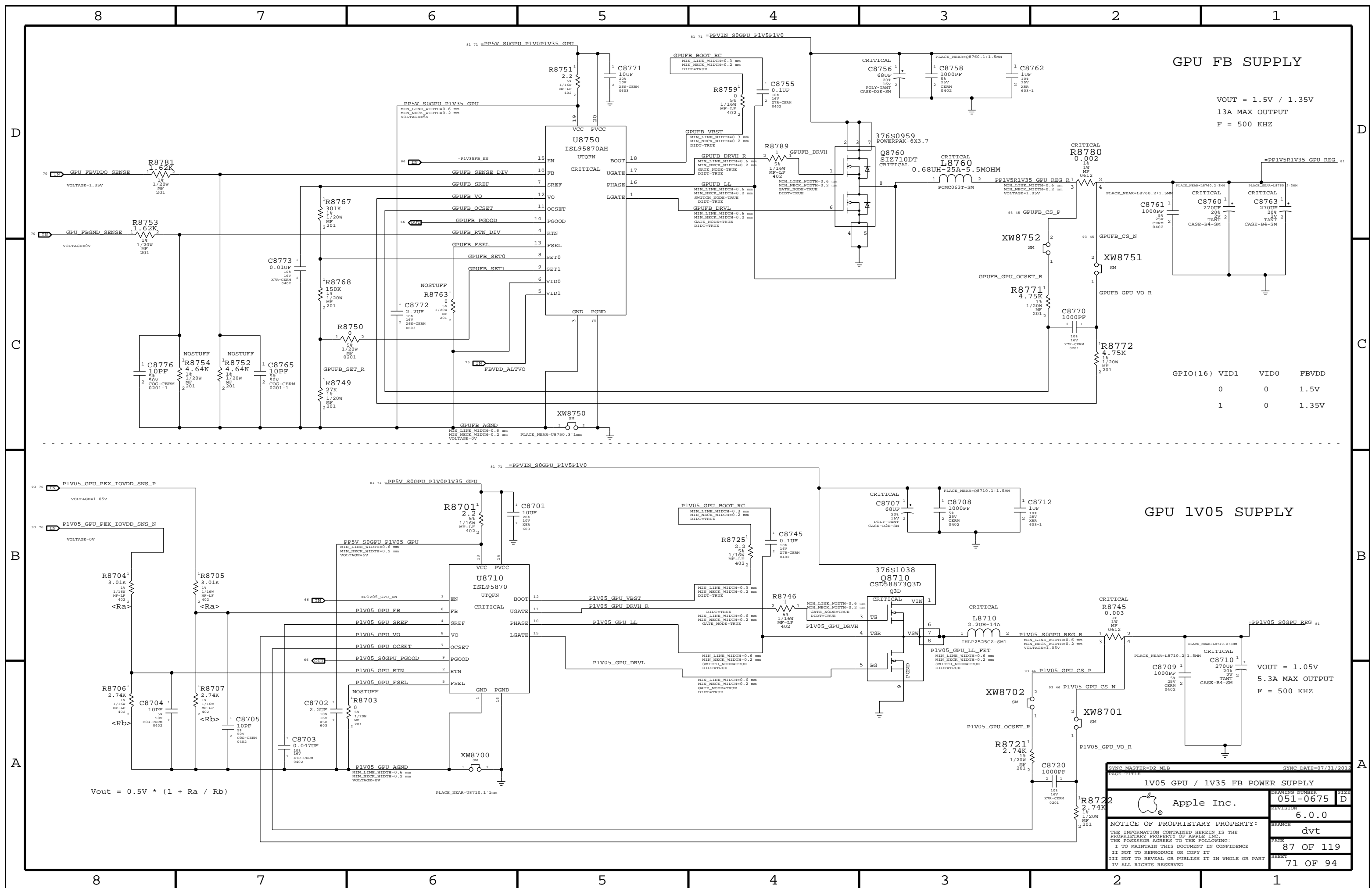
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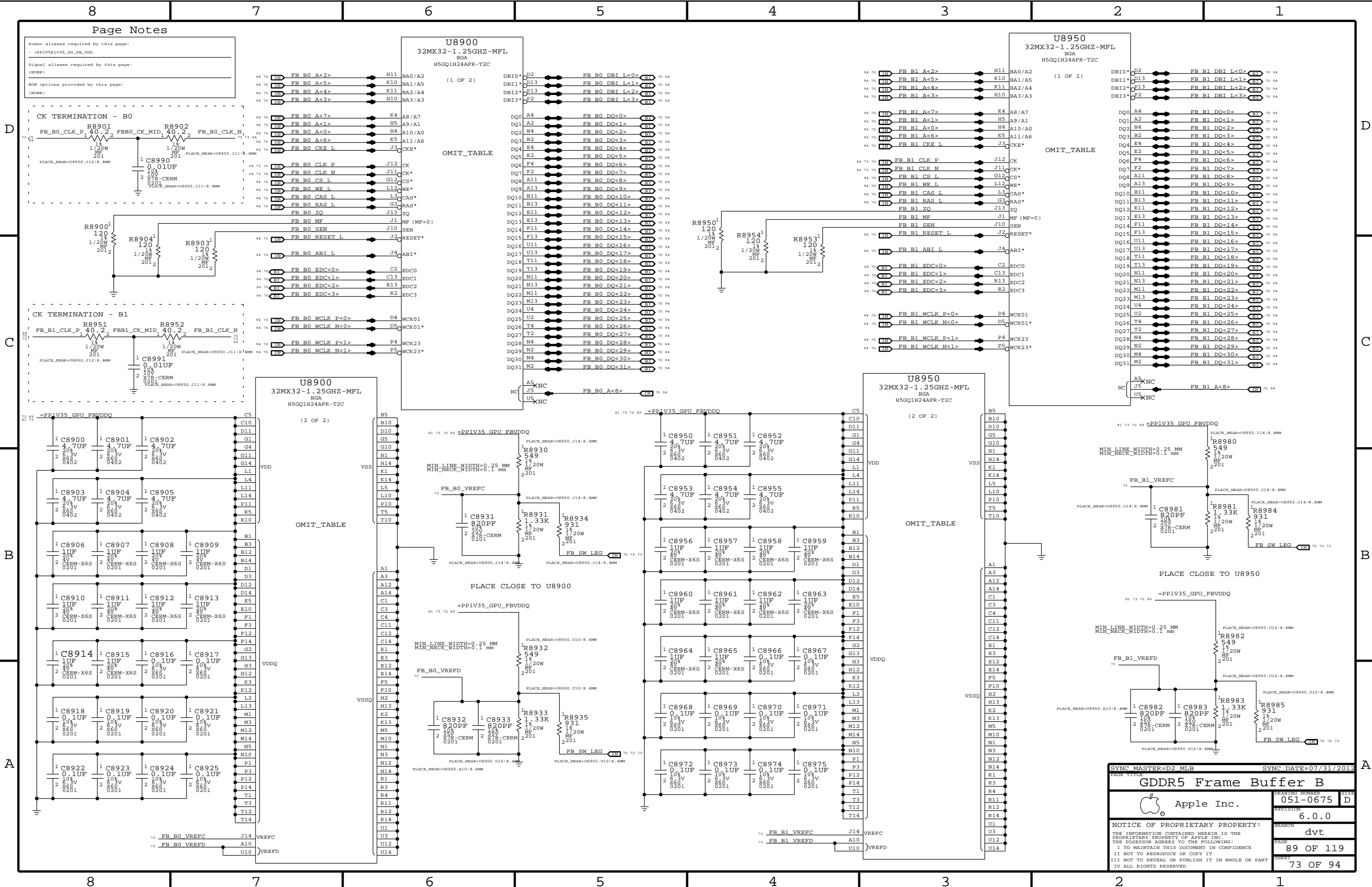


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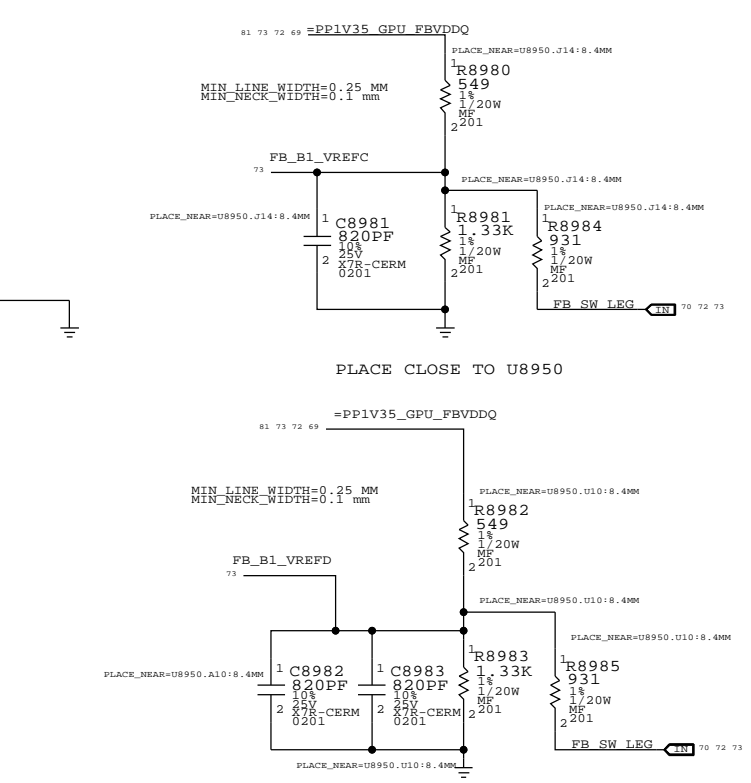
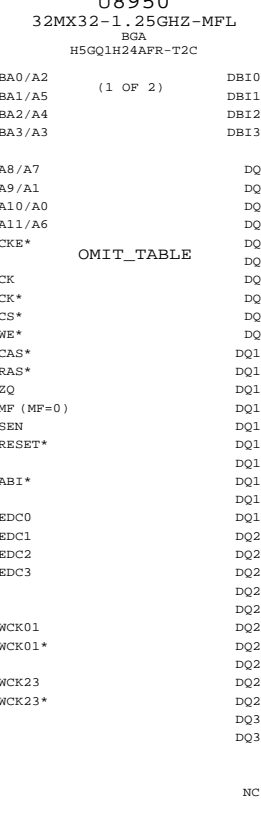
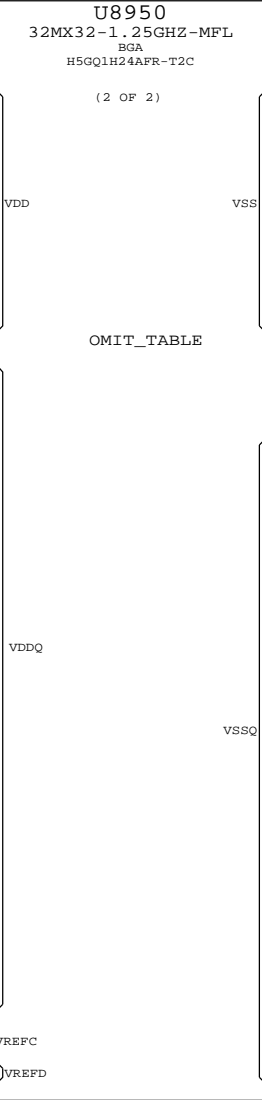
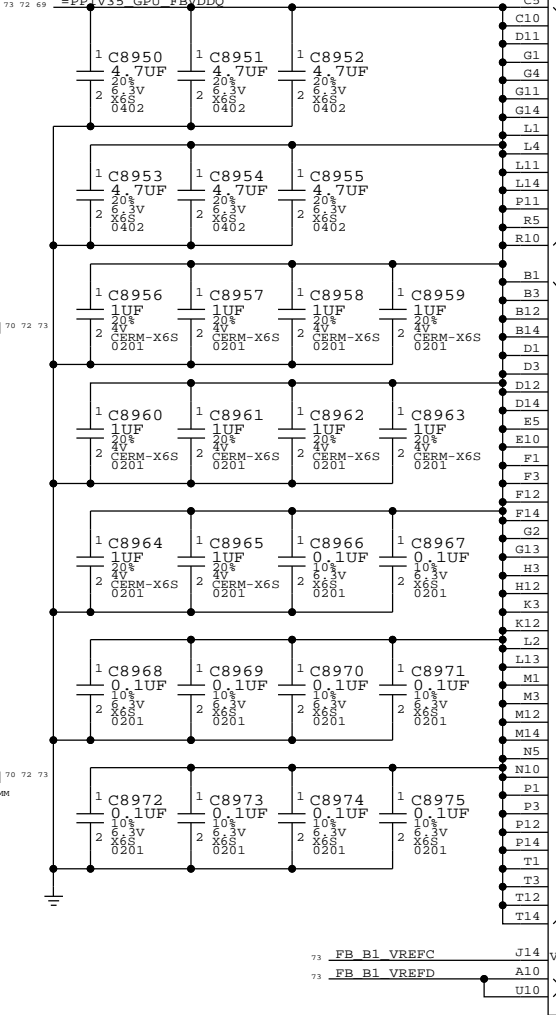
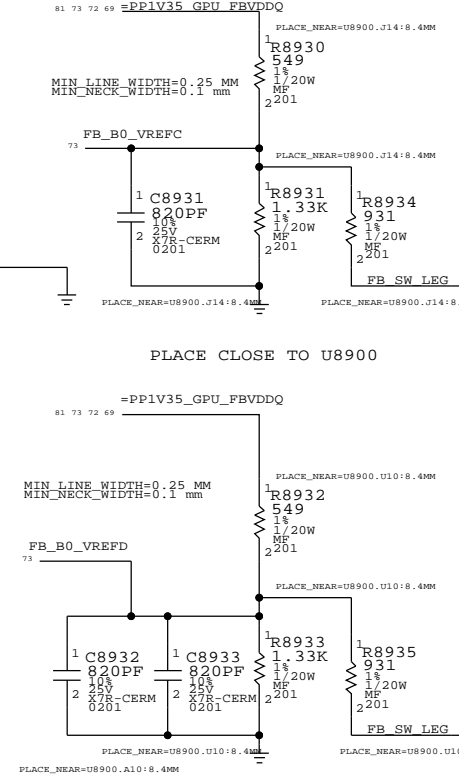
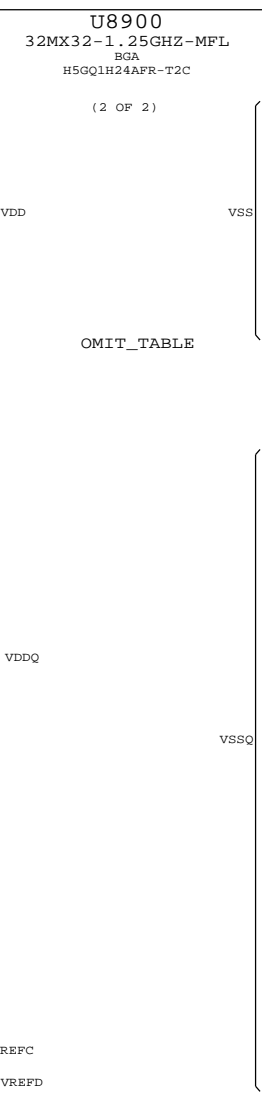
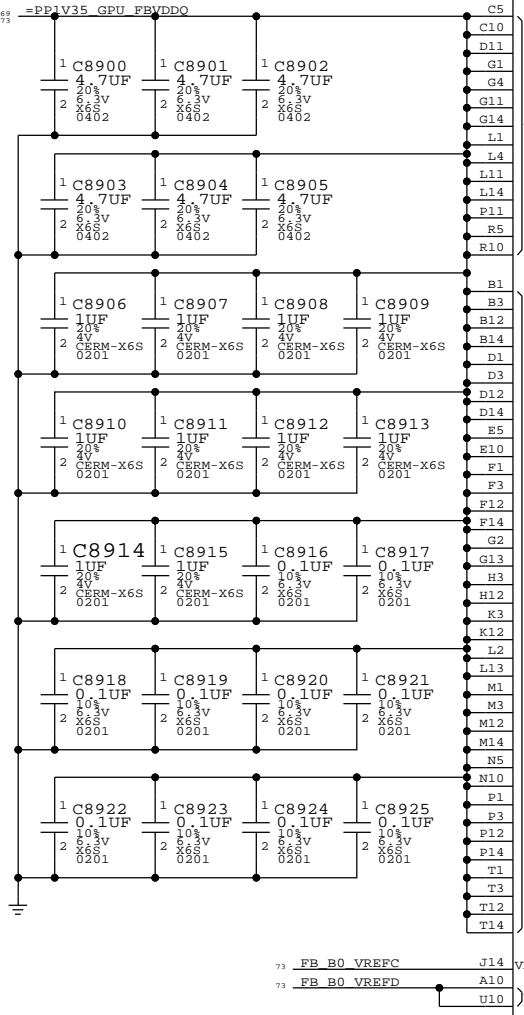
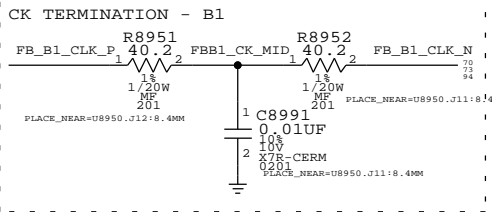
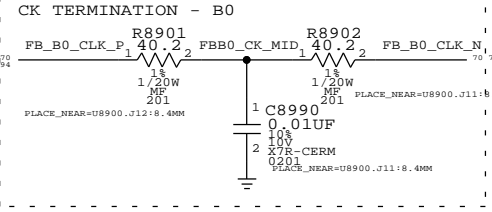





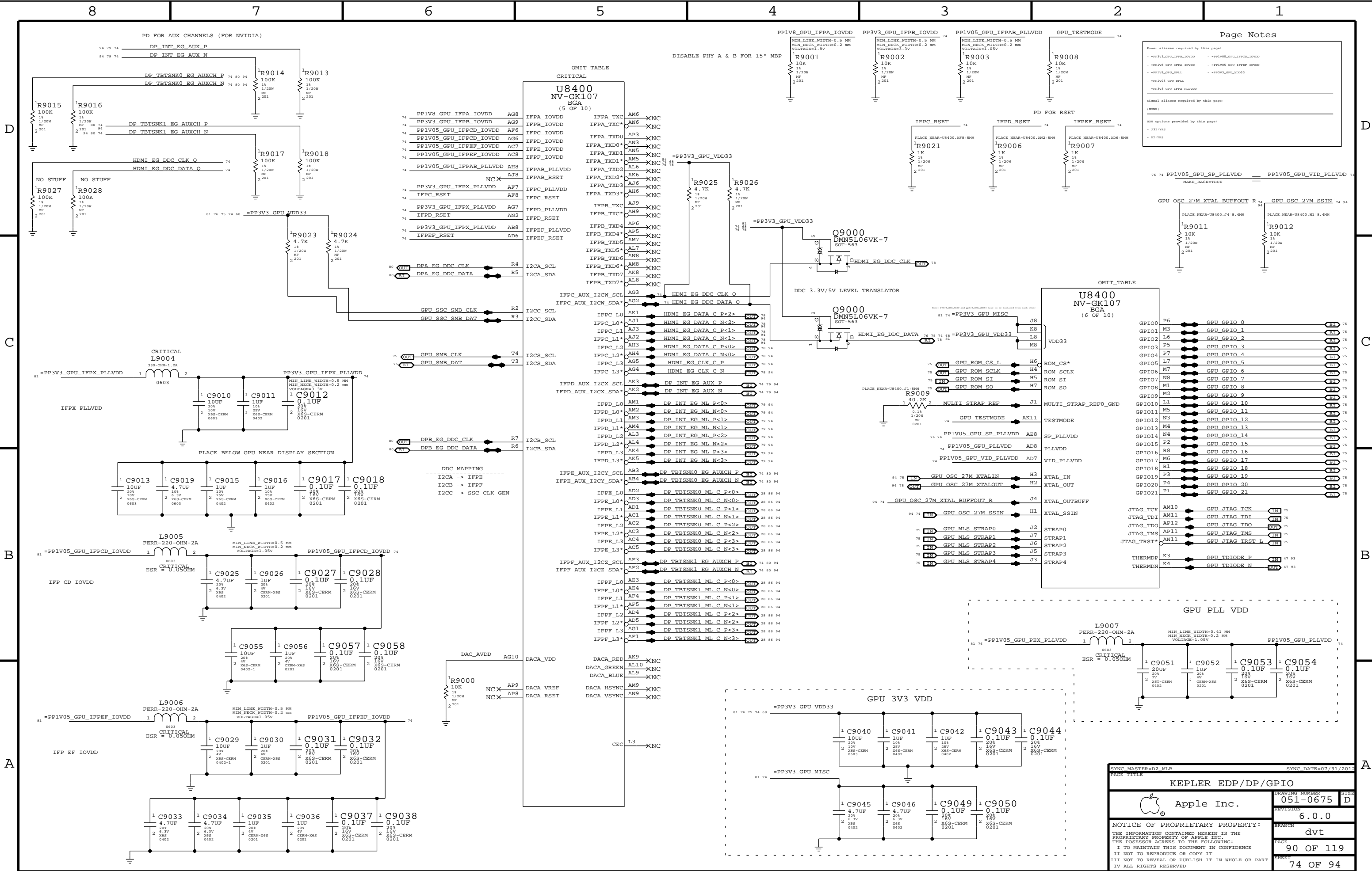
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Signal aliases required by this page:  
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BOM options provided by this page:  
(NONE)



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PAGE TITLE			
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	DRAWING NUMBER		SIZE
	051-0675		D
	REVISION		
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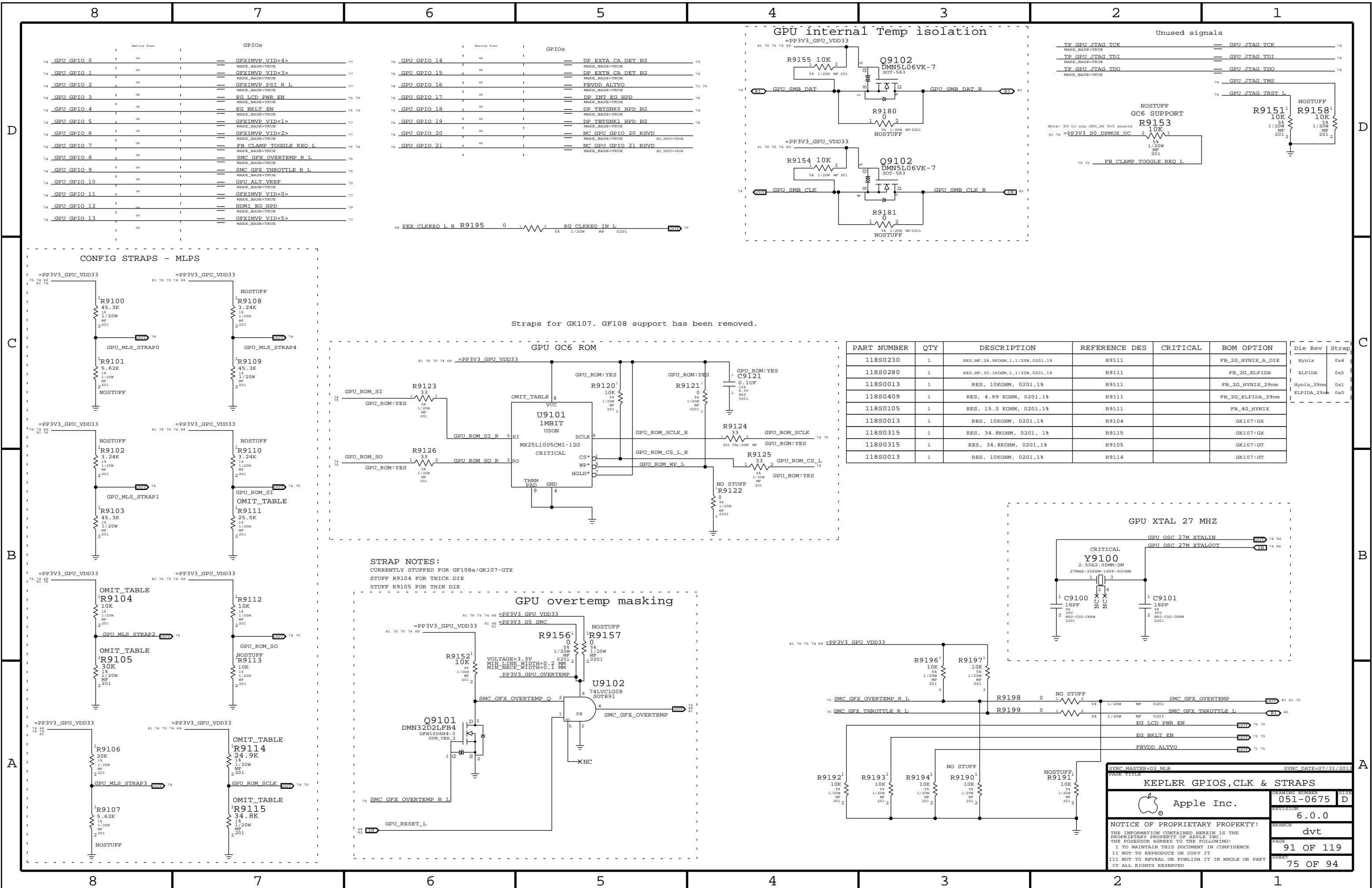
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- PP1V8\_GPU\_SPLL
- PP1V05\_GPU\_SPLL
- PP1V8\_GPU\_VDD33
- PP1V05\_GPU\_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- J311VBS
- D31VBS



D

C

B

A

D

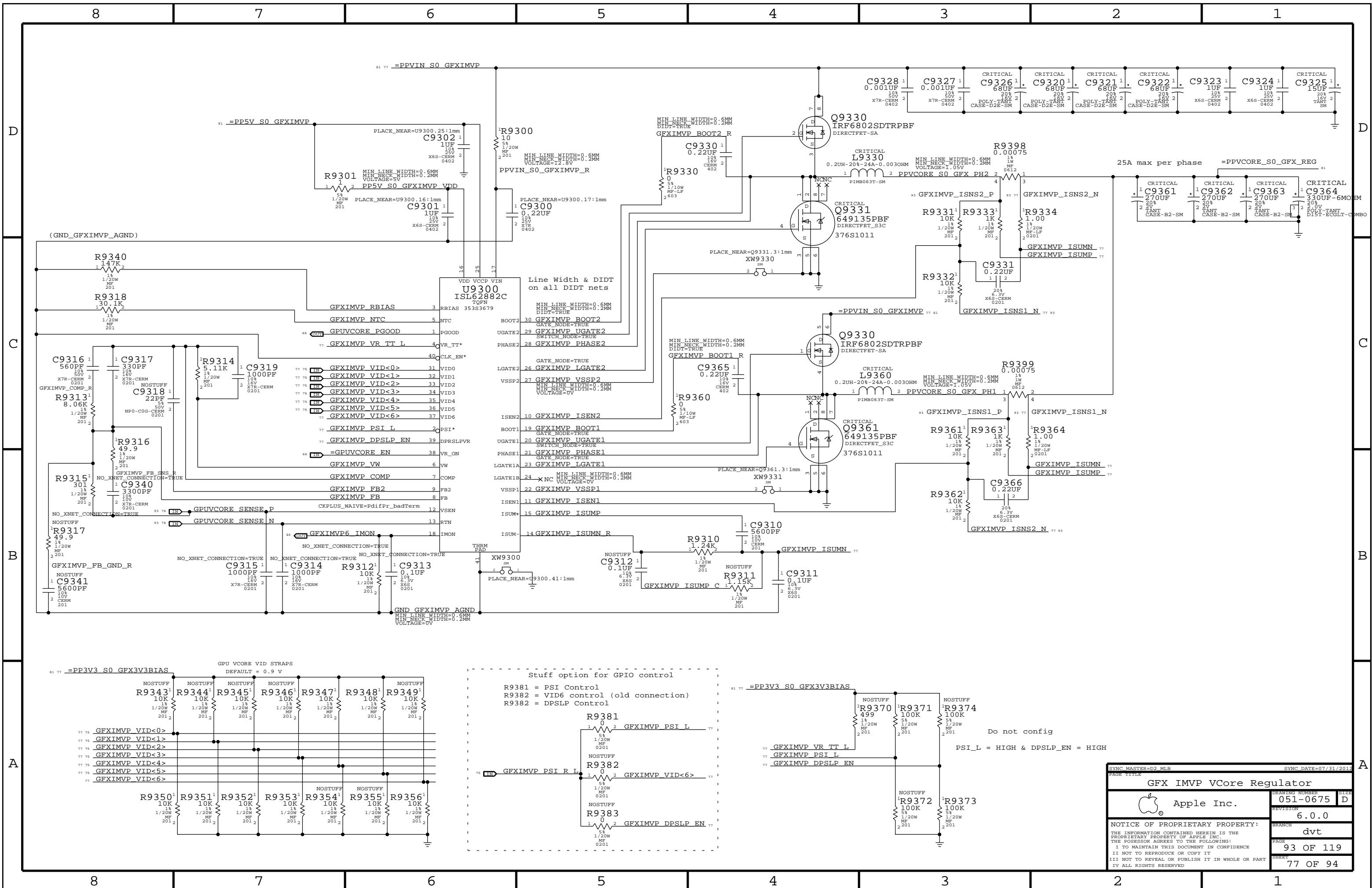
C


B

A



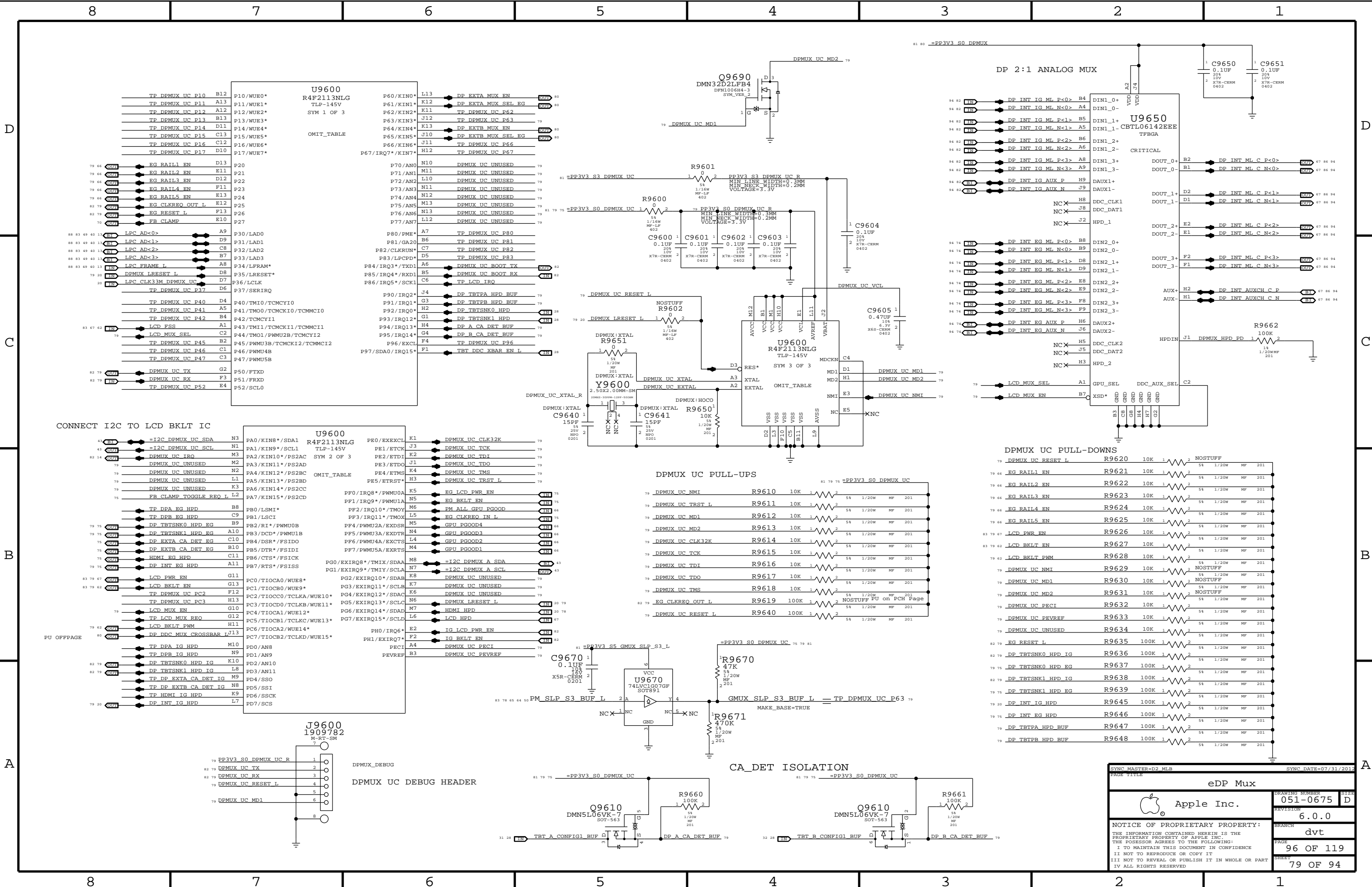


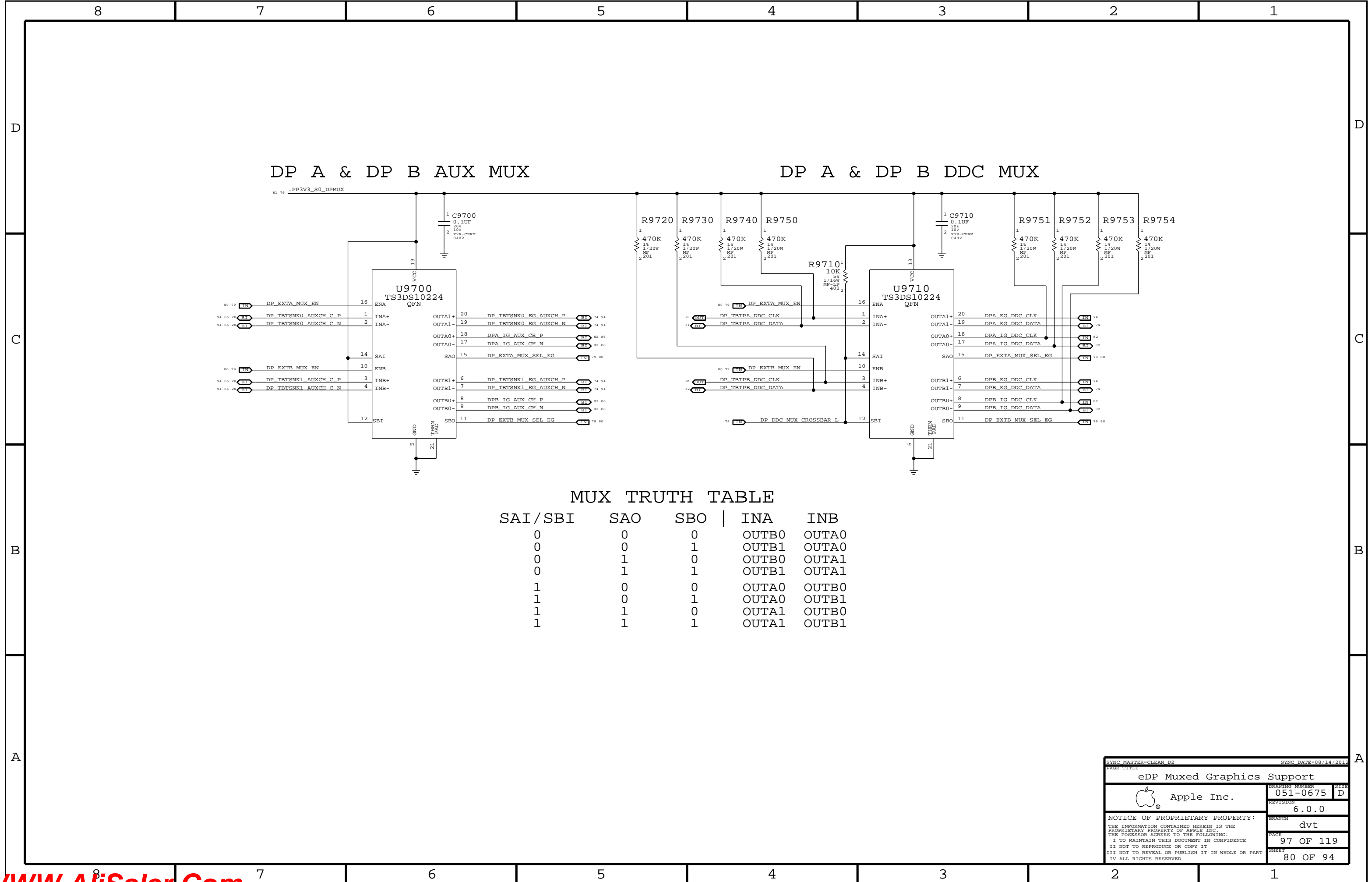


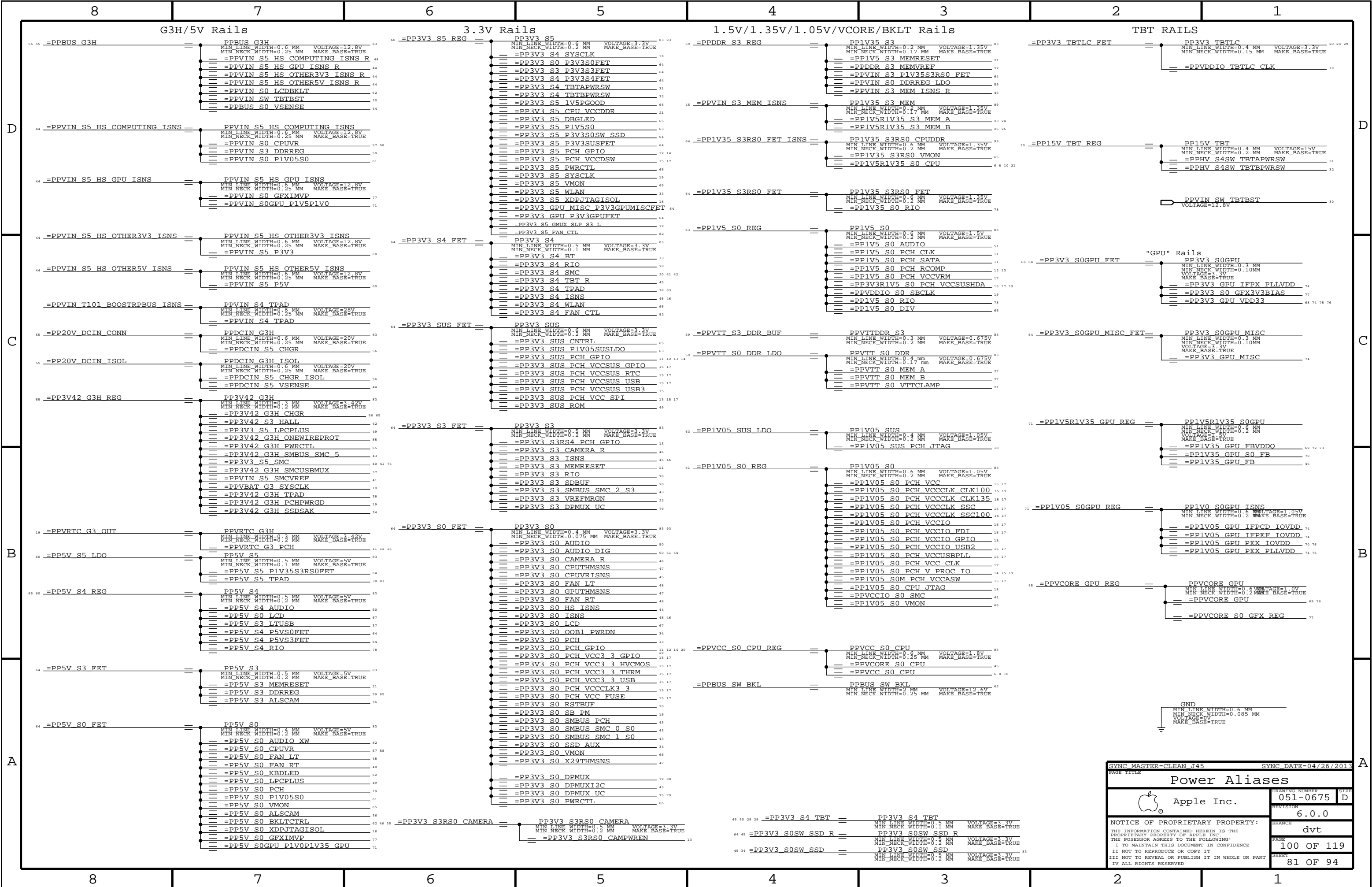
SYNC MASTER=D2 MLB		SYNC DATE=07/31/2012	
PAGE TITLE			
GFX IMVP VCore Regulator			
	DRAWING NUMBER		SIZE
	051-0675		D
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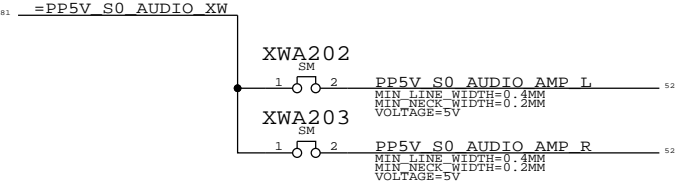
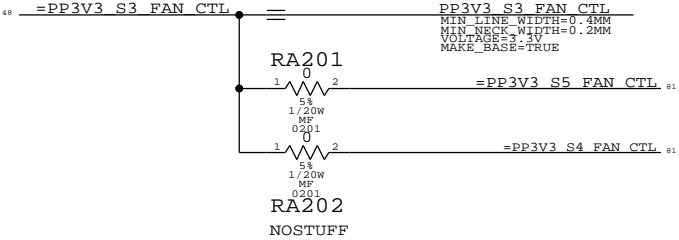




Display Aliases

12 EDP IG PANEL PWR == IG LCD PWR EN 79  
MAKE\_BASE=TRUE  
12 EDP IG BKL ON == IG BKLT EN 79  
MAKE\_BASE=TRUE  
94 79 DP INT IG ML P<3..0> == TP DP IG A MLP<3..0> 5  
MAKE\_BASE=TRUE  
94 79 DP INT IG ML N<3..0> == TP DP IG A MLN<3..0> 5  
MAKE\_BASE=TRUE  
94 79 DP INT IG AUX P == TP DP IG A AUXCHP 5  
MAKE\_BASE=TRUE  
94 79 DP INT IG AUX N == TP DP IG A AUXCHN 5  
MAKE\_BASE=TRUE  
86 80 DPA IG AUX CH P == TP DP IG B AUXCHP 12  
MAKE\_BASE=TRUE  
86 80 DPA IG AUX CH N == TP DP IG B AUXCHN 12  
MAKE\_BASE=TRUE  
86 80 DPB IG AUX CH P == TP DP IG C AUXCHP 12  
MAKE\_BASE=TRUE  
86 80 DPB IG AUX CH N == TP DP IG C AUXCHN 12  
MAKE\_BASE=TRUE  
80 DPA IG DDC CLK == TP DP IG B DDC CLK 12  
MAKE\_BASE=TRUE  
80 DPA IG DDC DATA == TP DP IG B DDC DATA 12  
MAKE\_BASE=TRUE  
80 DPB IG DDC CLK == TP DP IG C DDC CLK 12  
MAKE\_BASE=TRUE  
80 DPB IG DDC DATA == TP DP IG C DDC DATA 12  
MAKE\_BASE=TRUE  
79 DP TBTSNK0 HPD IG == TP DP IG B HPD 12  
MAKE\_BASE=TRUE  
79 DP TBTSNK1 HPD IG == TP DP IG C HPD 12  
MAKE\_BASE=TRUE  
79 DPMUX UC RX == DPMUX UC BOOT RX 79  
MAKE\_BASE=TRUE  
79 DPMUX UC TX == DPMUX UC BOOT TX 79  
MAKE\_BASE=TRUE  
79 EG RESET L == GPU RESET L 68 75  
MAKE\_BASE=TRUE  
82 11 PEG CLKREQ L == EG CLKREQ OUT L 79  
MAKE\_BASE=TRUE  
18 11 DP AUXCH ISOL L == DP AUXIO\_EN 79  
MAKE\_BASE=TRUE

PPVREF S3 MEM VREFDQ A == 0.675V TRUE PP0V75 S3 MEM VREFDQ A  
PPVREF S3 MEM VREFDQ B == 0.675V TRUE PP0V75 S3 MEM VREFDQ B  
PPVREF S3 MEM VREFCA A == 0.675V TRUE PP0V75 S3 MEM VREFCA A  
PPVREF S3 MEM VREFCA B == 0.675V TRUE PP0V75 S3 MEM VREFCA B



CPU signals

21 MEMVTT\_EN == =DDRVTT\_EN 21 59  
MAKE\_BASE=TRUE  
86 66 PEG D2R P<7..0> == =PEG D2R P<7..0> 5  
MAKE\_BASE=TRUE  
86 66 PEG D2R N<7..0> == =PEG D2R N<7..0> 5  
MAKE\_BASE=TRUE  
86 66 PEG R2D C P<7..0> == =PEG R2D C P<7..0> 5  
MAKE\_BASE=TRUE  
86 66 PEG R2D C N<7..0> == =PEG R2D C N<7..0> 5  
MAKE\_BASE=TRUE

NC PCIE PEG D2RP<15..12> == =PEG D2R P<15..12> 5  
MAKE\_BASE=TRUE NO\_TEST=TRUE  
NC PCIE PEG D2RN<15..12> == =PEG D2R N<15..12> 5  
MAKE\_BASE=TRUE NO\_TEST=TRUE  
NC PCIE PEG R2D CP<15..12> == =PEG R2D C P<15..12> 5  
MAKE\_BASE=TRUE NO\_TEST=TRUE  
NC PCIE PEG R2D CN<15..12> == =PEG R2D C N<15..12> 5  
MAKE\_BASE=TRUE NO\_TEST=TRUE

Thunderbolt Signals Through PEG

86 28 PCIE TBT D2R P<3..0> == =PEG D2R P<11..8> 5  
MAKE\_BASE=TRUE  
86 28 PCIE TBT D2R N<3..0> == =PEG D2R N<11..8> 5  
MAKE\_BASE=TRUE  
86 28 PCIE TBT R2D C P<3..0> == =PEG R2D C P<11..8> 5  
MAKE\_BASE=TRUE  
86 28 PCIE TBT R2D C N<3..0> == =PEG R2D C N<11..8> 5  
MAKE\_BASE=TRUE

88 83 68 PEG CLK100M N == TP PCIE CLK100M GPUN 11  
MAKE\_BASE=TRUE  
88 83 68 PEG CLK100M P == TP PCIE CLK100M GPUP 11  
MAKE\_BASE=TRUE

TP\_P1V8GPU\_EN\_ =P1V8GPU\_EN 66

Unused signals

BT PWRRST L  
MEM\_VDD\_SEL\_1V5\_L  
FW\_PWR\_EN\_PCH  
WOL\_EN  
FW\_PME\_L  
DP\_TBT\_SEL  
ENET\_MEDIA\_SENSE\_RDIV  
AUD\_IPHS\_SWITCH\_EN\_PCH  
AUD\_IP\_PERIPHERAL\_DET  
AUD\_I2C\_INT\_L  
TBT\_GO2SX\_BIDIR  
DPMUX\_UC\_IRO  
PEG\_CLKREQ\_L  
ENET\_CLKREQ\_L  
ENET\_LOW\_PWR\_PCH  
HDMITBTMUX\_SEL\_TBT  
SDCONN\_OC\_L

SYNC MASTER=CLEAN J45

SYNC DATE=04/26/2013

Signal Aliases

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Functional Test Points

J3501 - airport		
TRUE	AP CLKREQ O L	33
TRUE	AP RESET CONN L	33
TRUE	PCIE AP D2R PI N	33 88
TRUE	PCIE AP D2R PI P	33 88
TRUE	PCIE AP R2D N	33 88
TRUE	PCIE AP R2D P	33 88
TRUE	PCIE CLK100M AP CONN N	33 88
TRUE	PCIE CLK100M AP CONN P	33 88
TRUE	PCIE WAKE L	12 33 35 88
TRUE	PP3V3 S3RS4 BT F	33
TRUE	PP3V3 WLAN	33 41
TRUE	USB BT CONN N	33 87
TRUE	USB BT CONN P	33 87
TRUE	WIFI EVENT L	33 40 41
TRUE	GND	4X

J4002 - Camera		
TRUE	MIPI CLK CONN N	36 91
TRUE	MIPI CLK CONN P	36 91
TRUE	CAM SENSOR WAKE L CONN	36
TRUE	MIPI DATA CONN N	36 91
TRUE	MIPI DATA CONN P	36 91
TRUE	=I2C ALS SDA	36 43
TRUE	=I2C ALS SCL	36 43
TRUE	I2C CAM SCK	35 36
TRUE	I2C CAM SDA	35 36
TRUE	PP5V S3RS0 ALSCAM F	36
TRUE	GND	

J9500 - rio coax		
TRUE	HDMI CLK N	86
TRUE	HDMI CLK P	86
TRUE	HDMI DATA N<0>	86
TRUE	HDMI DATA N<1>	86
TRUE	HDMI DATA N<2>	86
TRUE	HDMI DATA P<0>	86
TRUE	HDMI DATA P<1>	86
TRUE	HDMI DATA P<2>	86

TRUE	USB3 SD D2R N	20 78 88
TRUE	USB3 SD D2R P	20 78 88
TRUE	USB3 SD R2D C N	20 78 88
TRUE	USB3 SD R2D C P	20 78 88
TRUE	USB3 EXTB D2R N	13 78 87
TRUE	USB3 EXTB D2R P	13 78 87
TRUE	USB3 EXTB R2D N	78 87
TRUE	USB3 EXTB R2D P	78 87
TRUE	USB EXTB N	13 78 87
TRUE	USB EXTB P	13 78 87
TRUE	GND	19X

J9510 - rio flex		
TRUE	SD PWR EN	13 18 78
TRUE	PP1V5R1V35 S0 RIO	78
TRUE	HDMI DDC CLK	
TRUE	HDMI DDC DATA	
TRUE	HDMI HPD L	
TRUE	SMBUS PCH CLK	13 43 88
TRUE	SMBUS PCH DATA	13 43 88
TRUE	PM SLP S3 BUF L	50 64 65 78 79
TRUE	PM SLP S4 L	12 21 33 37 40 65 78
TRUE	PP3V3 S3	3X 81 83
TRUE	PP3V3 S4	81 83
TRUE	PP5V S4	5X 81
TRUE	RIO SDCONN STATE CHANGE L	20 78
TRUE	USB EXTB OC L	18 78
TRUE	GND	10X

J5150 - hall effect		
TRUE	PP3V42 G3H	81 83
TRUE	SMC LID R	42
TRUE	GND	

J6050 - left fan		
TRUE	FAN LT PWM	48
TRUE	FAN LT TACH	48
TRUE	PP5V S0	3X 81 83
TRUE	GND	5X

J6060 - right fan		
TRUE	FAN RT PWM	48
TRUE	FAN RT TACH	48
TRUE	PP5V S0	3X 81 83
TRUE	GND	5X

J6100 - lpc + spi		
TRUE	LPCPLUS GPIO	14 49
TRUE	LPCPLUS RESET L	20 49
TRUE	LPC AD<0>	13 40 49 79 88
TRUE	LPC AD<1>	13 40 49 79 88
TRUE	LPC AD<2>	13 40 49 79 88
TRUE	LPC AD<3>	13 40 49 79 88
TRUE	LPC CLK33M LPCPLUS	19 49 88
TRUE	LPC FRAME L	13 40 49 79 88
TRUE	LPC PWRDWN L	12 20 40 49
TRUE	LPC SERIRO	13 40 49
TRUE	PM CLKRUN L	12 40 49
TRUE	PP5V S0	81 83
TRUE	SMC RESET L	40 41 49 56
TRUE	SMC ROMBOOT	41 49
TRUE	SMC RX L	40 41 49
TRUE	SMC TCK	40 41 49
TRUE	SMC TDI	40 41 49
TRUE	SMC TDO	40 41 49
TRUE	SMC TMS	40 41 49
TRUE	SMC TX L	40 41 49
TRUE	SPIROM USE MLB	14 49
TRUE	SPI ALT CLK	49
TRUE	SPI ALT CS L	49
TRUE	SPI ALT MISO	49
TRUE	SPI ALT MOSI	49
TRUE	TP SMC MD1	49
TRUE	TP SMC TRST L	49
TRUE	GND	2X

J4800 - ipd flex		
TRUE	Z2 CS L	38
TRUE	Z2 MOSI	38
TRUE	Z2 MISO	38
TRUE	Z2 SCLK	38
TRUE	Z2 HOST INTN	38
TRUE	Z2 CLKIN	38
TRUE	Z2 KEY ACT L	38
TRUE	PSOC F CS L	38
TRUE	PICKB L	38
TRUE	PSOC MOSI	38
TRUE	PSOC MISO	38
TRUE	PSOC SCLK	38
TRUE	=I2C TPAD SCL	38 43
TRUE	=I2C TPAD SDA	38 43
TRUE	SMC LID	38 40 41 42
TRUE	SMC T101 COM 1	
TRUE	=PP3V3 S4 TPAD	38 81
TRUE	=PP5V S5 TPAD	38 81
TRUE	GND	2X

J4813 - keyboard		
TRUE	PP3V3 S4	81 83
TRUE	PP3V42 G3H	81 83
TRUE	WS CONTROL KBD	38
TRUE	WS KBD1	38
TRUE	WS KBD10	38
TRUE	WS KBD11	38
TRUE	WS KBD12	38
TRUE	WS KBD13	38
TRUE	WS KBD14	38
TRUE	WS KBD15 CAP	38
TRUE	WS KBD16 NUM	38
TRUE	WS KBD17	38
TRUE	WS KBD18	38
TRUE	WS KBD19	38
TRUE	WS KBD2	38
TRUE	WS KBD20	38
TRUE	WS KBD21	38
TRUE	WS KBD22	38
TRUE	WS KBD23	38
TRUE	WS KBD3	38
TRUE	WS KBD4	38
TRUE	WS KBD5	38
TRUE	WS KBD6	38
TRUE	WS KBD7	38
TRUE	WS KBD8	38
TRUE	WS KBD9	38
TRUE	WS KBD ONOFF L	38
TRUE	WS LEFT OPTION KBD	38
TRUE	WS LEFT SHIFT KBD	38
TRUE	GND	2X

J4915 - kbd bklt		
TRUE	KBDBKLT RETURN1	2X 39 62
TRUE	KBDBKLT RETURN2	2X 39 62
TRUE	PPVOUT S0 KBDBKLT	39 62
TRUE	GND	4X

J6701 - audio flex		
TRUE	AUD HP PORT L	50 54
TRUE	AUD HP PORT R	50 54
TRUE	AUD SPDIF OUT JACK	
TRUE	AUD TIPDET INV	
TRUE	AUD TYPEDET	50 54
TRUE	AUD CONN MIC XW	4X
TRUE	CH HS MIC	
TRUE	PP3V3 S0	81 83 93
TRUE	AUD CONN SLEEVE XW	4X 53 54
TRUE	US HS MIC	
TRUE	GND	2X GND

J6601 - mic		
TRUE	DMIC CLK3	51 54
TRUE	PP3V3 S0	81 83 93
TRUE	DMIC SDA2	54
TRUE	DMIC SDA3	51 54
TRUE	GND	

J6602 - L speaker		
TRUE	SPKRCONN L ID	51 54
TRUE	SPKRCONN L OUT N	52 54 93
TRUE	SPKRCONN L OUT P	52 54 93
TRUE	SPKRCONN SL OUT N	52 54 93
TRUE	SPKRCONN SL OUT P	52 54 93
TRUE	GND	

J6603 - R speaker		
TRUE	SPKRCONN R ID	51 54
TRUE	SPKRCONN R OUT N	52 54 93
TRUE	SPKRCONN R OUT P	52 54 93
TRUE	SPKRCONN SR OUT N	52 54 93
TRUE	SPKRCONN SR OUT P	52 54 93
TRUE	GND	

J7000 - DC PWR		
TRUE	ADAPTER SENSE	55
TRUE	PP20V DCIN FUSE	2X 55
TRUE	GND	2X

J7050 - battery		
TRUE	PPVBAT G3H CONN	8X 55 56
TRUE	SMBUS SMC 5 G3 SCL	40 43 92
TRUE	SMBUS SMC 5 G3 SDA	40 43 92
TRUE	SYS DETECT L	55
TRUE	GND	8X

J8300 - eDP		
TRUE	DP INT AUX N	67 86 94
TRUE	DP INT AUX P	67 86 94
TRUE	DP INT ML N<0>	67 86 94
TRUE	DP INT ML N<1>	67 86 94
TRUE	DP INT ML N<2>	67 86 94
TRUE	DP INT ML N<3>	67 86 94
TRUE	DP INT ML P<0>	67 86 94
TRUE	DP INT ML P<1>	67 86 94
TRUE	DP INT ML P<2>	67 86 94
TRUE	DP INT ML P<3>	67 86 94
TRUE	LCD FSS	62 67 79
TRUE	LCD HPD CONN	67
TRUE	LED RETURN 1	62 67
TRUE	LED RETURN 2	62 67
TRUE	LED RETURN 3	62 67
TRUE	LED RETURN 4	62 67
TRUE	LED RETURN 5	62 67
TRUE	LED RETURN 6	62 67
TRUE	PP5VR3V3 SW LCD	3X 67
TRUE	PPVOUT S0 LCDBKLT	62 67
TRUE	GND	16X

Power Rails		
TRUE	PM SLP S3 L	12 21 40 65
TRUE	PPVTT S0 DDR	81
TRUE	PP3V3 S0	81 83 93
TRUE	PP3V3 S3	81 83
TRUE	PP3V3 S5	81 93
TRUE	PP3V3 S5 AVREF SMC	40 41
TRUE	PP3V42 G3H	81 83
TRUE	PP5V S0	81 83
TRUE	PP5V S3	81
TRUE	PP5V S5	81
TRUE	PPBUS G3H	81
TRUE	PPDCIN G3H	81
TRUE	PPVCC S0 CPU	81
TRUE	PPVTDDR S3	81
TRUE	PP3V3 S0SW SSD	81
TRUE	PP1V5 S0	81
TRUE	PP1V35 S3	81

XDP		
TRUE	XDP CPU TCK	6 18 86
TRUE	XDP PCH TCK	11 18
TRUE	XDP CPU TDI	6 18 86
TRUE	XDP CPU TDO	6 18 86
TRUE	XDP CPU TRST L	6 18 86
TRUE	XDP CPU TMS	6 18 86
TRUE	XDP PCH TMS	11 18
TRUE	XDP PCH TDI	11 18
TRUE	XDP PCH TDO	11 18
TRUE	XDP CPU PREQ L	6 18 86
TRUE	XDP CPU PRDY L	6 18 86
TRUE	PM RSMRST L	12 65 88
TRUE	PM PCH PWROK	12 19 88
TRUE	PM SYSRST L	12 19 40 88
TRUE	CRU CFG<3>	6 18 86
TRUE	PP1V05 S0	81
TRUE	GND	2X GND

Power Sequence		
TRUE	SMC ONOFF L	38 40 41
TRUE	PM DSW PWRGD	12 40 88
TRUE	ALL SYS PWRGD	18 19 40 65
TRUE	PM PCH SYS PWROK	12 18 19 40 88
TRUE	PLT RESET L	12 18 20 21
TRUE	LCD PWR EN	67 79
TRUE	LCD BKLT EN	62 79

TPA401	PEG CLK100M P	68 82 88
TPA402	PEG CLK100M N	68 82 88

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
Functional Test Points			
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## NC NO\_TESTS

PCH

NO\_TEST MAKE\_BASE

10	TP_USB3_SPARE_D2RN	==	TRUE	TRUE	NC_USB3_SPARE_D2RN
10	TP_USB3_SPARE_D2RP	==	TRUE	TRUE	NC_USB3_SPARE_D2RP
10	TP_USB3_SPARE_R2D_CN	==	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
10	TP_USB3_SPARE_R2D_CP	==	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
10	USB3_EXTC_D2R_N	==	TRUE	TRUE	NC_USB3_EXTC_D2R_N
10	USB3_EXTC_D2R_P	==	TRUE	TRUE	NC_USB3_EXTC_D2RP
10	USB3_EXTC_R2D_C_N	==	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
10	USB3_EXTC_R2D_C_P	==	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
10	USB3_EXTD_D2R_N	==	TRUE	TRUE	NC_USB3_EXTD_D2RN
10	USB3_EXTD_D2R_P	==	TRUE	TRUE	NC_USB3_EXTD_D2RP
10	USB3_EXTD_R2D_C_N	==	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
10	USB3_EXTD_R2D_C_P	==	TRUE	TRUE	NC_USB3_EXTD_R2D_CP

PCIE ENET D2RN	—	TRUE	TRUE	NC	PCIE ENET D2RN
PCIE ENET D2RP	—	TRUE	TRUE	NC	PCIE ENET D2RP
PCIE ENET R2D CN	—	TRUE	TRUE	NC	PCIE ENET R2D CN
PCIE ENET R2D CP	—	TRUE	TRUE	NC	PCIE ENET R2D CP

11	SATA A D2R N	==	TRUE	TRUE	NC SATA A D2RN	87
11	SATA A D2R P	==	TRUE	TRUE	NC SATA A D2RP	87
11	SATA A R2D C N	==	TRUE	TRUE	NC SATA A R2D CN	87
11	SATA A R2D C P	==	TRUE	TRUE	NC SATA A R2D CP	87
11	SATA B D2R N	==	TRUE	TRUE	NC SATA B D2RN	87
11	SATA B D2R P	==	TRUE	TRUE	NC SATA B D2RP	87
11	SATA B R2D C N	==	TRUE	TRUE	NC SATA B R2D CN	87
11	SATA B R2D C P	==	TRUE	TRUE	NC SATA B R2D CP	87
11	TP SATA ODD D2RN	==	TRUE	TRUE	NC SATA ODD D2RN	87
11	TP SATA ODD D2RP	==	TRUE	TRUE	NC SATA ODD D2RP	87
11	TP SATA ODD R2D CN	==	TRUE	TRUE	NC SATA ODD R2D CN	87
11	TP SATA ODD R2D CP	==	TRUE	TRUE	NC SATA ODD R2D CP	87
11	TP SATA D D2RN	==	TRUE	TRUE	NC SATA D D2RN	87
11	TP SATA D D2RP	==	TRUE	TRUE	NC SATA D D2RP	87
11	TP SATA D R2D CN	==	TRUE	TRUE	NC SATA D R2D CN	87
11	TP SATA D R2D CP	==	TRUE	TRUE	NC SATA D R2D CP	87
11	TP SATA F D2RN	==	TRUE	TRUE	NC SATA F D2RN	87
11	TP SATA F D2RP	==	TRUE	TRUE	NC SATA F D2RP	87
11	TP SATA F R2D CN	==	TRUE	TRUE	NC SATA F R2D CN	87
11	TP SATA F R2D CP	==	TRUE	TRUE	NC SATA F R2D CP	87

11	USB_EXTC_N	==	TRUE	TRUE	NC_USB_EXTCN	87
13	USB_EXTC_P	==	TRUE	TRUE	NC_USB_EXTCP	87
13	TP_USB_SDN	==	TRUE	TRUE	NC_USB_SDN	87
13	TP_USB_SDP	==	TRUE	TRUE	NC_USB_SDP	87
13	TP_USB_WLANN	==	TRUE	TRUE	NC_USB_WLANN	87
13	TP_USB_WLANP	==	TRUE	TRUE	NC_USB_WLANP	87
13	TP_USB_6N	==	TRUE	TRUE	NC_USB_6N	87
13	TP_USB_6P	==	TRUE	TRUE	NC_USB_6P	87
13	TP_USB_7N	==	TRUE	TRUE	NC_USB_7N	87
13	TP_USB_7P	==	TRUE	TRUE	NC_USB_7P	87
13	USB_EXTD_N	==	TRUE	TRUE	NC_USB_EXTDN	87
13	USB_EXTD_P	==	TRUE	TRUE	NC_USB_EXTDP	87
13	TP_USB_PSOCN	==	TRUE	TRUE	NC_USB_PSOCN	87
13	TP_USB_PSOC_P	==	TRUE	TRUE	NC_USB_PSOC_P	87
13	USB_IR_N	==	TRUE	TRUE	NC_USB_IRN	87
13	USB_IR_P	==	TRUE	TRUE	NC_USB_IRP	87

86	1	ITPXPDP CLK100M N	==	TRUE	TRUE	NC ITPXPDP CLK100MN
86	1	ITPXPDP CLK100M P	==	TRUE	TRUE	NC ITPXPDP CLK100MP
		TP PCI PME L	==	TRUE	TRUE	NC PCI PME L
20	1	TP PCI CLK33M OUT2	==	TRUE	TRUE	NC PCI CLK33M OUT2
		TP PCI CLK33M OUT3	==	TRUE	TRUE	NC PCI CLK33M OUT3
		TP HDA SDIN1	==	TRUE	TRUE	NC HDA SDIN1
11	1	TP HDA SDIN2	==	TRUE	TRUE	NC HDA SDIN2
11	1	TP HDA SDIN3	==	TRUE	TRUE	NC HDA SDIN3
13	1	TP LPC DREQ0 L	==	TRUE	TRUE	NC LPC DREQ0 L
		TP CLINK CLK	==	TRUE	TRUE	NC CLINK CLK
		TP CLINK DATA	==	TRUE	TRUE	NC CLINK DATA
		TP CLINK RESET L	==	TRUE	TRUE	NC CLINK RESET L

12	EDP	IG	BKL	PWM	—	TRUE	TRUE	NC	EDP	IG	BKL	PWM
----	-----	----	-----	-----	---	------	------	----	-----	----	-----	-----

87	<u>USB SMC P</u>	<u>—</u>	<u>TRUE</u>	<u>TRUE</u>	<u>NC USB SMC P</u>
87	<u>USB SMC N</u>	<u>—</u>	<u>TRUE</u>	<u>TRUE</u>	<u>NC USB SMC N</u>

---

SMC INTERFACE 2                      — TRUE           TRUE           NC SMC INTERFACE 2

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Thunderbolt

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NO_TEST MAKE_BASE
```

```

28 TP_TBT_XTAL25OUT      — TRUE      TRUE      NC_TBT_XTAL25OUT

```

28	TP	DP	TBTSRC	ML	CP<3..0>	=	TRUE	TRUE	NC	DP	TBTSRC	ML	CP<3..0>
28	TP	DP	TBTSRC	ML	CN<3..0>	=	TRUE	TRUE	NC	DP	TBTSRC	ML	CN<3..0>
28	TP	DP	TBTSRC	AUXCH	CP	=	TRUE	TRUE	NC	DP	TBTSRC	AUXCH	CP
28	TP	DP	TBTSRC	AUXCH	CN	=	TRUE	TRUE	NC	DP	TBTSRC	AUXCH	CN

12	TP	DP	IG	D	AUXCHN	=	TRUE	TRUE	NC	DP	IG	D	AUXCHN
12	TP	DP	IG	D	AUXCHP	=	TRUE	TRUE	NC	DP	IG	D	AUXCHP

11	TP	PCIE	CLK100M	PE5N	---	TRUE	TRUE	NC	PCIE	CLK100M	PE5N
12	TP	PCIE	CLK100M	PE5P	---	TRUE	TRUE	NC	PCIE	CLK100M	PE5P
13	PCIE	CLK100M	ENETSD	N	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETSDN
14	PCIE	CLK100M	ENETSD	P	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETSDP
15	TP	PCIE	CLK100M	ENETN	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETN
16	TP	PCIE	CLK100M	ENETP	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETP
17	TP	PCIE	CLK100M	PEGBN	---	TRUE	TRUE	NC	PCIE	CLK100M	PEGBN
18	TP	PCIE	CLK100M	PEGBP	---	TRUE	TRUE	NC	PCIE	CLK100M	PEGBP
19	TP	PCIE	CLK100M	SWN	---	TRUE	TRUE	NC	PCIE	CLK100M	SWN
20	TP	PCIE	CLK100M	SWP	---	TRUE	TRUE	NC	PCIE	CLK100M	SWP

11	TP_PCH_GPIO64_CLKOUTFLEX0	=	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
11	TP_PCH_GPIO65_CLKOUTFLEX1	=	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
11	TP_PCH_GPIO66_CLKOUTFLEX2	=	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
11	TP_PCH_GPIO67_CLKOUTFLEX3	=	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

13	<u>TP USB 4N</u>	<u>=</u>	TRUE	TRUE	NC USB 4N
13	<u>TP USB 4P</u>	<u>=</u>	TRUE	TRUE	NC USB 4P

TRUE	PCIE TBT R2D P<3..0>	28 86
TRUE	PCIE TBT R2D N<3..0>	28 86
TRUE	PCIE TBT D2R C P<3..0>	28 86
TRUE	PCIE TBT D2R C N<3..0>	28 86

R19	TRUE	DMI S2N P<3..1>	5	12	86
R19	TRUE	DMI S2N N<3..1>	5	12	86
R19	TRUE	DMI N2S P<3..1>	5	12	86
R19	TRUE	DMI N2S N<3..1>	5	12	86

PLACEABLE BEAD-PROBES FOR TBT

```

90 31 28      TBT A R2D C P<1>          1  TDSM BEAD-PROBE BPA535 NO_XNET_CONNECTION=TRUE
90 31 28      TBT A D2R P<1>          1  TDSM BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
90 31 28      TBT A D2R N<1>          1  TDSM BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

```



## J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE_ADJ	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE_ADJ	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	TEL3, TEL4, TEL9, TEL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

## Stackup-Defined Spacing Rules


Note: Outer dielectric is 0.058 mm nominal,  
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1X_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL1, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2N2S	*	=6X_DIELECTRIC	?	DMICKLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2S2N	*	=3X_DIELECTRIC	?	DMICKLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKLK2OTHER	*	=4X_DIELECTRIC	?	DMICKLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKLK2N2S
CLK_DMI	DMI_S2N	*	DMICKLK2S2N
CLK_DMI	*	*	DMICKLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?	PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICKLK_2CLK	*	=7x_DIELECTRIC	?	HDMICKLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICKLK_2DP	*	=4x_DIELECTRIC	?	HDMICKLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICKLK_2OTHER	*	=7x_DIELECTRIC	?	HDMICKLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICKLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICKLK_2DP
HDMI_CLK	*	*	HDMICKLK_2OTHER

DisplayPort/TMDs intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.  
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.  
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.  
MAX LENGTH OF DISPLAYPORT/TMDs TRACES: 13 INCHES.

CPU Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 84
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 84
FDI_INT	CPU_50S	CPU_AGTL	FDI INT	5 12
FDI_CSVMC	CPU_50S	CPU_AGTL	FDI CSVMC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI CLK100M CPU P	4 11
DMI_CLK	CPU_85D	CLK_DMI	DMI CLK100M CPU N	4 11
CPU_CLK135_PL1	CPU_85D	CLK_PCIE	CPU CLK135M DPLLREF N	6 11
CPU_CLK135_PL1	CPU_85D	CLK_PCIE	CPU CLK135M DPLLREF P	6 11
CPU_CLK135_PL1	CPU_85D	CLK_PCIE	CPU CLK135M DPLLSS N	6 11
CPU_CLK135_PL1	CPU_85D	CLK_PCIE	CPU CLK135M DPLLSS P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU EDP RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU PEG RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU CFG<19..0>	6 18 83
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP CLK100M P	11 84
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP CLK100M N	11 84
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI	6 18 83
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO	6 18 83
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS	6 18 83
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK	6 18 83
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CPU TRST_L	6 18 83
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP BPM L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP CPU PRDY_L	6 18 83
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP CPU PREQ_L	6 18 83
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU Peci	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT_L	6 40 41 57
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_SMII	PM THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM MEM PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU VIDSOUT	8 57
CPU_VID	CPU_45S	CPU_VID	CPU VIDCLK	8 57
CPU_VID	CPU_45S	CPU_VID	CPU VIDALERT_L	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	9 57
CPU_MEM_VREF		CPU_VREF	CPU DIMMA VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU DIMMB VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PPVREF S3 MEM VREFDQ A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF S3 MEM VREFDQ B	22 25 26 82
CPU_MEM_VREF		MEM_PWR	PPVREF S3 MEM VREFCA A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF S3 MEM VREFCA B	22 25 26 82
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R P<7..0>	46 68 82
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R N<7..0>	46 68 82
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R C P<7..0>	46
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R C N<7..0>	46
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D P<7..0>	46 68
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D N<7..0>	46 68
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D C P<7..0>	48 82
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D C N<7..0>	48 82
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R P<3..0>	28 82
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R N<3..0>	28 82
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R C P<3..0>	28 84
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R C N<3..0>	28 84
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D P<3..0>	28 84
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D C P<3..0>	28 82
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D C N<3..0>	28 82

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>	67 79 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>	67 79 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0>	67 83 86 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0>	67 83 86 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F P<3..0>	67 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F N<3..0>	67 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0>	67 83 86 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0>	67 83 86 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C P	67 79 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C N	67 79 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP INT AUX P	67 83 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP INT AUX N	67 83 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA IG AUX CH P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA IG AUX CH N	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DEB IG AUX CH P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DEB IG AUX CH N	80 82

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA P<2..0>	83
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA N<2..0>	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK P	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK N	83
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>	28 74 94
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>	28 74 94
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>	28 94
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>	28 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>	28 74 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>	28 74 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>	28 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>	28 94
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH P	28 94
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH N	28 94
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH C P	28 80 94
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH C N	28 80 94
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH P	28 94
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH N	28 94
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH C P	28 80 94
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH C N	28 80 94

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CPU Constraints			
 Apple Inc.		DRAWING NUMBER	051-0675
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### SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

### USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

### USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

### System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?


NOTE: 25MHz system clocks very sensitive to noise.  
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

### PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
NC SATA A R2D_CP	SATA_R5D	SATA_R2D	84
NC SATA A R2D_CN	SATA_R5D	SATA_R2D	84
NC SATA A D2RP	SATA_R5D	SATA_D2R	84
NC SATA A D2RN	SATA_R5D	SATA_D2R	84
NC SATA B R2D_CP	SATA_R5D	SATA_R2D	84
NC SATA B R2D_CN	SATA_R5D	SATA_R2D	84
NC SATA B D2RP	SATA_R5D	SATA_D2R	84
NC SATA B D2RN	SATA_R5D	SATA_D2R	84
PCH SATA RCOMP	SATA_45SE	SATA_RCOMP	11
USB_EXT_A_P	USB_85D	USB	13 37
USB_EXT_A_N	USB_85D	USB	13 37
USB_EXT_A_MUXED_P	USB_85D	USB	37
USB_EXT_A_MUXED_N	USB_85D	USB	37
USB_LT1_P	USB_85D	USB	37
USB_LT1_N	USB_85D	USB	37
NC USB_EXTCP	USB_85D	USB	84
NC USB_EXTCN	USB_85D	USB	84
NC USB_SDP	USB_85D	USB	84
NC USB_SDN	USB_85D	USB	84
SMC_DEBUGPRT_RX_L	CPU_45S	CPU_ITP	37 40 41
SMC_DEBUGPRT_TX_L	CPU_45S	CPU_ITP	37 40 41
USB_SMC_P	USB_85D	USB	84
USB_SMC_N	USB_85D	USB	84
NC USB_6P	USB_85D	USB	84
NC USB_6N	USB_85D	USB	84
NC USB_7P	USB_85D	USB	84
NC USB_7N	USB_85D	USB	84
USB_EXTB_P	USB_85D	USB	13 78 83
USB_EXTB_N	USB_85D	USB	13 78 83
NC USB_EXTRDP	USB_85D	USB	84
NC USB_EXTRDN	USB_85D	USB	84
USB_BT_P	USB_85D	USB	13 33
USB_BT_N	USB_85D	USB	13 33
USB_BT_CONN_P	USB_85D	USB	33 83
USB_BT_CONN_N	USB_85D	USB	33 83
NC USB_IRP	USB_85D	USB	84
NC USB_IRN	USB_85D	USB	84
USB_TPAD_P	USB_85D	USB	13 38
USB_TPAD_N	USB_85D	USB	13 38
USB_TPAD_R_P	USB_85D	USB	38
USB_TPAD_R_N	USB_85D	USB	38
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	13
USB3_EXT_A_D2R_P	USB_85D	USB3_D2R	13 37
USB3_EXT_A_D2R_N	USB_85D	USB3_D2R	13 37
USB3_EXT_A_D2R_C_P	USB_85D	USB3_D2R	13 37
USB3_EXT_A_D2R_C_N	USB_85D	USB3_D2R	13 37
USB3_EXT_A_R2D_P	USB_85D	USB3_R2D	37
USB3_EXT_A_R2D_N	USB_85D	USB3_R2D	37
USB3_EXT_A_R2D_C_P	USB_85D	USB3_R2D	13 37
USB3_EXT_A_R2D_C_N	USB_85D	USB3_R2D	13 37
USB3_EXTB_D2R_P	USB_85D	USB3_D2R	13 78 83
USB3_EXTB_D2R_N	USB_85D	USB3_D2R	13 78 83
USB3_EXTB_D2R_C_P	USB_85D	USB3_D2R	13 78 83
USB3_EXTB_D2R_C_N	USB_85D	USB3_D2R	13 78 83
USB3_EXTB_R2D_P	USB_85D	USB3_R2D	78 83
USB3_EXTB_R2D_N	USB_85D	USB3_R2D	78 83
USB3_EXTB_R2D_C_P	USB_85D	USB3_R2D	13 78
USB3_EXTB_R2D_C_N	USB_85D	USB3_R2D	13 78
NC_USB3_EXTC_D2RP	USB_85D	USB3_D2R	84
NC_USB3_EXTC_D2RN	USB_85D	USB3_D2R	84
NC_USB3_EXTC_R2D_CP	USB_85D	USB3_R2D	84
NC_USB3_EXTC_R2D_CN	USB_85D	USB3_R2D	84
NC_USB3_EXTD_D2RP	USB_85D	USB3_D2R	84
NC_USB3_EXTD_D2RN	USB_85D	USB3_D2R	84
NC_USB3_EXTD_R2D_CP	USB_85D	USB3_R2D	84
NC_USB3_EXTD_R2D_CN	USB_85D	USB3_R2D	84

### Clock Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	11 19
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	11 19
SYSCLK_CLK25M_SB_R	CLK_25M_45S	CLK_25M	11
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	19 36
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	19 28
SYSCLK_CLK25M_TBT_R	CLK_25M_45S	CLK_25M	28

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PCH Constraints 1			
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## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	= 2x_DIELECTRIC	?

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

## PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?	PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

## PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SV_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

## PCH Net Properties

ELECTRICAL_CONSTRAINT		SET	PHYSICAL	SPACING	NET_TYPE	
	LPC_AD		LPC_45S	LPC	LPC_AD<3..0>	13 40 49 79 83
	LPC_FRAME_L		LPC_45S	LPC	LPC_FRAME_L	13 40 49 79 83
	LPC_RESET_L		LPC_45S	LPC	LPC_RESET_L	20
	SMBUS_PCH_CLK		SMR_45S	SMR	SMBUS_PCH_CLK	13 43 83
	SMBUS_PCH_DATA		SMR_45S	SMR	SMBUS_PCH_DATA	13 43 83
	SMBUS_PCH_0_CLK		SMR_45S	SMR	SML_PCH_0_CLK	13 43
	SMBUS_PCH_0_DATA		SMR_45S	SMR	SML_PCH_0_DATA	13 43
	SMBUS_PCH_1_CLK		SMR_45S	SMR	SML_PCH_1_CLK	13 43
	SMBUS_PCH_1_DATA		SMR_45S	SMR	SML_PCH_1_DATA	13 43
	HDA_BIT_CLK		HDA_45S	HDA	HDA_BIT_CLK	11 51
			HDA_45S	HDA	HDA_BIT_CLK_R	11
	HDA_SYNC		HDA_45S	HDA	HDA_SYNC	11 51
			HDA_45S	HDA	HDA_SYNC_R	11
			HDA_45S	HDA	HDA_RST_R_L	11
	HDA_RST_L		HDA_45S	HDA	HDA_RST_L	11 51
	HDA_SDIN0		HDA_45S	HDA	HDA_SDIN0	11 51
	HDA_SDIN0_R		HDA_45S	HDA	CS4208_HDA_SDOU0_R	51
	HDA_SDOU0		HDA_45S	HDA	HDA_SDOU0	11 51
			HDA_45S	HDA	HDA_SDOU0_R	11 19
	SPT_CLK		SPT_45S	SPT	SPI_CLK_R	13 49
			SPT_45S	SPT	SPI_CLK	49
			SPT_45S	SPT	SPI_MOSI_R	13 49
	SPT_MOSI		SPT_45S	SPT	SPI_MOSI	49
	SPT_MISO		SPT_45S	SPT	SPI_MISO	13 49
			SPT_45S	SPT	SPI_CS0_R_L	13 49
	SPT_CS0		SPT_45S	SPT	SPI_CS0_L	49
	USB3_SD_R2D		USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	20 78 83
	USB3_SD_R2D		USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	20 78 83
	USB3_SD_D2R		USB3_85D	USB3_D2R	USB3_SD_D2R_P	20 78 83
	USB3_SD_D2R		USB3_85D	USB3_D2R	USB3_SD_D2R_N	20 78 83
	PCIE_AP_R2D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	33 83
	PCIE_AP_R2D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	33 83
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 33
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 33
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	33
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	33
	PCIE_AP_D2R		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 33
	PCIE_AP_D2R		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 33
	PCIE_85D		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	33 83
	PCIE_85D		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	33 83
	PCIE_CAMERA_R2D		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	35 36
	PCIE_CAMERA_R2D		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	35 36
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 36
	PCIE_85D		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 36
	PCIE_CAMERA_D2R		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 36
	PCIE_CAMERA_D2R		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 36
	PCIE_85D		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	35 36
	PCIE_85D		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	35 36
	CLK_LPC_45S		CLK_LPC		LPC_CLK33M_SMC_R	11 19
	CLK_LPC_45S		CLK_LPC		LPC_CLK33M_SMC	19 40
	CLK_LPC_45S		CLK_LPC		LPC_CLK33M_LPCPLUS	19 49 83
	CLK_LPC_45S		CLK_LPC		LPC_CLK33M_LPCPLUS_R	11 19
	PCIE_CLK100M		CPU_45S	CLK_PCIE	PCH_CLK33M_PCIEIN	11 19
	PCIE_CLK100M		CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
	PCIE_CLK100M		CPU_45S	CLK_PCIE	PCH_CLK33M_PCIEOUT	11 19
	PCIE_CLK100M_PCIE		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
	PCIE_CLK100M_PCIE		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
	PCIE_CLK100M_TBT		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
	PCIE_CLK100M_TBT		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
	PCIE_CLK100M_DOT		CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
	PCIE_CLK100M_DOT		CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
	PCIE_CLK100M_SATA		PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
	PCIE_CLK100M_SATA		PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
	PEG_CLK100M		PEG_80D	CLK_PCIE	PEG_CLK100M_P	68 82 83
	PEG_CLK100M		PEG_80D	CLK_PCIE	PEG_CLK100M_N	68 82 83
	PCIE_CLK100M_AP		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 33
	PCIE_CLK100M_AP		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 33
	PCIE_85D		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	33 83
	PCIE_85D		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	33 83
	PCIE_CLK100M_S2		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 36
	PCIE_CLK100M_S2		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 36
	PCIE_85D		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	35 36
	PCIE_85D		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	35 36
	PCIE_CLK100M_ENET		PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 34
	CLK_PCIE_85D		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 34

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
<b>H030</b>	PCH_EM_NET	PCH_45S	PCH_SF	PCH_INTRUDER_L	11
<b>H031</b>	PCH_EM_NET	PCH_45S	PCH_SF	PCH_INTVRMEN_L	11
<b>H032</b>	PCH_EM_NET	PCH_45S	PCH_SF	PCH_DSWVRMEN	12
<b>H033</b>	PCH_EM_NET	PCH_45S	PCH_SF	PCH_SRTCRST_L	11
<b>H034</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_RSMRST_L	12 65 83
<b>H035</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_SYSRST_L	12 19 40 83
<b>H036</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_PCH_PWROK	12 19 83
<b>H037</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_PCH_APWROK	12 19
<b>H038</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_DSW_PWRGD	12 40 83
<b>H039</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_PCH_SYS_PWROK	12 18 19 40 83
<b>H040</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_PWRBTN_L	12 18 40
<b>H041</b>	PCH_EM_NET	PCH_45S	PCH_SF	PM_THRMTRIP_L_R	14 41
<b>H042</b>	PCH_PCIE_WAKE	PCH_45S	PCH_SF	PCIE_WAKE_L	12 33 35 83
<b>H043</b>	PCH_EM_NET	PCH_45S	PCH_SF	PCH_RCIN_L	14
<b>H044</b>	PCIE_D2R_SSD	PCIE_R5D	PCIE_D2R	PCIE_SSD D2R P<3..0>	13 34
<b>H045</b>	PCIE_D2R_SSD	PCIE_R5D	PCIE_D2R	PCIE_SSD D2R N<3..0>	13 34
<b>H046</b>	PCIE_R2D_SSD	PCIE_R5D	PCIE_R2D	PCIE_SSD R2D C P<3..0>	13 34
<b>H047</b>	PCIE_R2D_SSD	PCIE_R5D	PCIE_R2D	PCIE_SSD R2D C N<3..0>	13 34
<b>H048</b>		PCIE_R5D	PCIE_R2D	PCIE_SSD R2D P<3..0>	34
<b>H049</b>		PCIE_R5D	PCIE_R2D	PCIE_SSD R2D N<3..0>	34

## Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

## Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

## Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

### DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair  
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.  
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].  
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.  
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.  
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.  
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.  
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down  
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

## Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

## Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM A CLK P<0>	7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM A CLK N<0>	7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM A CLK P<1>	7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM A CLK N<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A CKE<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A CKE<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A CS L<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A CS L<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A ODT<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A ODT<1>	7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM A DQS P<0>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM A DQS N<0>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM A DQS P<1>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM A DQS N<1>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM A DQS P<2>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM A DQS N<2>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM A DQS P<3>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM A DQS N<3>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM A DQS P<4>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM A DQS N<4>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM A DQS P<5>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM A DQS N<5>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM A DQS P<6>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM A DQS N<6>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM A DQS P<7>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM A DQS N<7>	7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM B CLK P<0>	7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM B CLK N<0>	7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM B CLK P<1>	7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM B CLK N<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B CKE<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B CKE<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B CS L<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B CS L<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B ODT<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B ODT<1>	7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM B DQS P<0>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM B DQS N<0>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM B DQS P<1>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM B DQS N<1>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM B DQS P<2>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM B DQS N<2>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM B DQS P<3>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM B DQS N<3>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM B DQS P<4>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM B DQS N<4>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM B DQS P<5>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM B DQS N<5>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM B DQS P<6>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM B DQS N<6>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM B DQS P<7>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM B DQS N<7>	7 25 26
		MEM_PWR	PPVREF S3 MEM VREFDQ A	22 23 24 82 86
		MEM_PWR	PPVREF S3 MEM VREFCA A	22 23 24 82 86
		MEM_PWR	PP1V35 S3 MEM	81

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PAGE TITLE			
Memory Constraints			
 Apple Inc.		DRAWING NUMBER	051-0675
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT\_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C P<1..0> 28 31 84
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C N<1..0> 28 31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D P<1..0> 31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D N<1..0> 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1> 28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1> 28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1> 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1> 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1> 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1> 31
	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3> 28 31
	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3> 28 31
	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3> 31
	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3> 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<0> 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<0> 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R P<0> 28 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R N<0> 28 31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<1> 31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<1> 31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R P<1> 28 31 84
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R N<1> 28 31 84
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC P 31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC N 31
	TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C P 28 31
	TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C N 28 31
	TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH P 31
	TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH N 31


	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C P<1..0> 28 32
	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C N<1..0> 28 32
	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D P<1..0> 32
	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D N<1..0> 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1> 28 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1> 28 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<1> 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<1> 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1> 32
	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1> 32
	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3> 28 32
	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3> 28 32
	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<3> 32
	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<3> 32
	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<0> 32
	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<0> 32
	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R P<0> 28 32
	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R N<0> 28 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<1> 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<1> 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R P<1> 28 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R N<1> 28 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC P 32
	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC N 32
	TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C P 28 32
	TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C N 28 32
	TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH P 32
	TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
		DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
		DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
		DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
	TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK 28
	TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI 28
	TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO 28
	TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L 28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

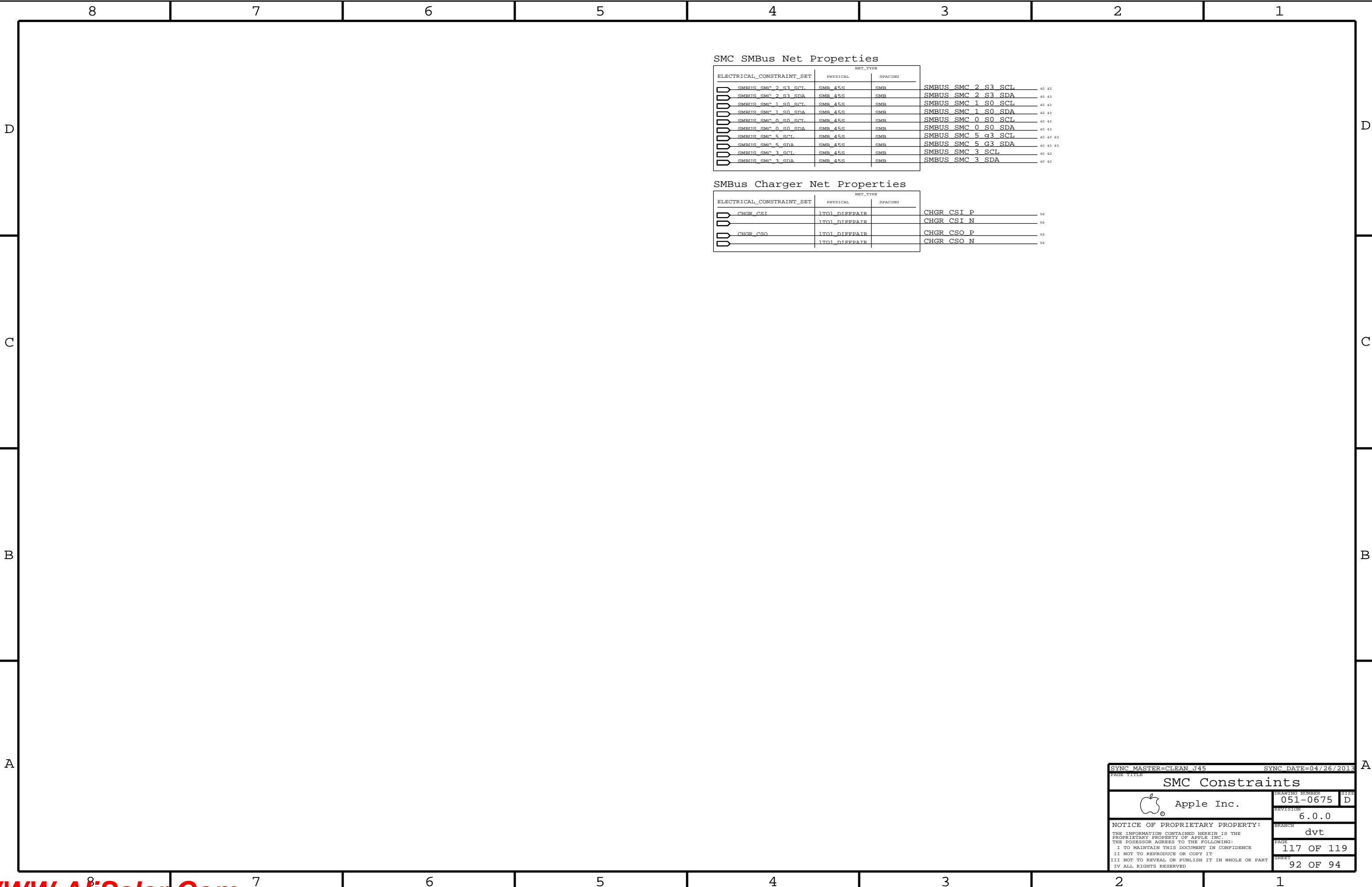
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 35 36
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 35 36
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 36 83
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 36 83
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 36 83
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 36 83
		S2_MEM_PWR	PP1V35_CAM 35 36
		S2_MEM_PWR	PP0V675_CAM_VREF 35 36
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 36
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 36

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_S3_SCL	40 43 83
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_S3_SDA	40 43 83
SMBUS_SMC_3_SCL	SMB_45S	SMB	SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1T01_DIEFPAIR		CHGR_CSI_P	56
	1T01_DIEFPAIR		CHGR_CSI_N	56
CHGR_CSO	1T01_DIEFPAIR		CHGR_CSO_P	56
	1T01_DIEFPAIR		CHGR_CSO_N	56

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_50S	*	+1:1_DIFFPAIR	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1T01_50S	*	+1:1_DIFFPAIR	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
AUDIODIFF	*	+1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	0.2 MM	0.2 MM
THERM_1T01_45S	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
SENSE_1T01_45S	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2X_DIELECTRIC	?
THERM	*	+2X_DIELECTRIC	?
AUDIO	*	+2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	+STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P20M
CPU_VCCSENSE	GND	*	GND_P20M

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P20M
GND	PCI_E*	*	GND_P20M
GND	SATA_*	*	GND_P20M
USB	GND	*	GND_P20M
CLK_PCIE	SB_POWER	*	PWR_P20M
SB_POWER	SATA_*	*	PWR_P20M
USB	SB_POWER	*	PWR_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_72D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_37S	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_85D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
PCIE_85D	*	OVERWRITE	OVERWRITE	0.09 MM	10 MM	OVERWRITE	OVERWRITE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1T01_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPUDDR_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPUDDR_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPU_DDR_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPU_DDR_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUTHMSNS_D2_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUTHMSNS_D2_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_LCD_PANEL_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_LCD_PANEL_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	DDR3THMSNS_D1_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	DDR3THMSNS_D1_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GPUTHMSNS_D_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GPUTHMSNS_D_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_R_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_R_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_GPUFB_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_GPUFB_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GPUFB_CS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GPUFB_CS_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER5V_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER5V_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER3V3_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER3V3_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	PLV05_GPU_CS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	PLV05_GPU_CS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_GPU_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_GPU_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR_ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR_ISNS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_PP1V0_S0GPU_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_PP1V0_S0GPU_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05_GPU_PEX_IOVDD_SNS_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05_GPU_PEX_IOVDD_SNS_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUVR_ISUM_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUVR_ISUM_R_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GFXIMVP_ISNS2_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GFXIMVP_ISNS2_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GFXIMVP_ISNS1_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GFXIMVP_ISNS1_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_N
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P
AUDIO_DIFFPAIR	AUDIO	AUDIO	ISNS_TBT_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_CS_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_CS_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_SENSE_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_SENSE_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_R_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_R_N

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_HS_MIC_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_HS_MIC_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	HS_MIC_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	HS_MIC_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	SB_POWER		PP1V35_S3RS0_CPUDDR
	GND		GND

SYNC MASTER=CLEAN J45

SYNC DATE=04/26/2013

Project Specific Constraints

Apple Inc.

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DRAWING NUMBER

051-0675

REVISION

6.0.0

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## GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

## GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE			
		PHYSICAL	SIGNAL		
PH00	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P	70 72
PH00	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N	70 72
PH00	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P	70 72
PH00	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 <8...0>	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 <8...0>	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 ABI L	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 ABI L	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 RAS L	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 RAS L	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CAS L	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CAS L	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 WE L	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 WE L	70 72
PH00	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 CKE L	70 72
PH00	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 CKE L	70 72
PH00	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CS L	70 72
PH00	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CS L	70 72
PH00	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>	70 72
PH00	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>	70 72
PH00	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>	70 72
PH00	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>	70 72
PH00	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>	70 72
PH00	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>	70 72
PH00	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>	70 72
PH00	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>	70 72
PH00	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>	70 72
PH00	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>	70 72
PH00	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>	70 72
PH00	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>	70 72
PH00	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>	70 72
PH00	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>	70 72
PH00	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>	70 72
PH00	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>	70 72
PH00	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>	70 72
PH00	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>	70 72
PH00	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>	70 72
PH00	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>	70 72
PH00	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>	70 72
PH00	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>	70 72
PH00	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>	70 72
PH00	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>	70 72
PH00	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7...0>	70 72
PH00	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15...8>	70 72
PH00	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23...16>	70 72
PH00	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31...24>	70 72
PH00	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7...0>	70 72
PH00	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15...8>	70 72
PH00	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23...16>	70 72
PH00	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31...24>	70 72
PH00	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 RESET L	70 72
PH00	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 RESET L	70 72

## GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET		INST_TYPE	
		PHYSICAL	SPACING
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 A<8..0>
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 A<8..0>
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 ABI L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 ABI L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 RAS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 RAS L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CAS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CAS L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 WE L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 WE L
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 CKE L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 CKE L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CS L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 RESET L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 RESET L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		REV: 0001	REV: 0001
		REV: 0001	REV: 0001
DP INT ML C P<3..0>	DP 85D	DISPLAYPORT	67 79 86
DP INT ML C N<3..0>	DP 85D	DISPLAYPORT	67 79 86
DP INT ML F P<3..0>	DP 85D	DISPLAYPORT	67 86
DP INT ML F N<3..0>	DP 85D	DISPLAYPORT	67 86
DP INT ML P<3..0>	DP 85D	DISPLAYPORT	67 83 86
DP INT ML N<3..0>	DP 85D	DISPLAYPORT	67 83 86
DP INT AUXCH C P	DP 85D	DISPLAYPORT	67 79 86
DP INT AUXCH C N	DP 85D	DISPLAYPORT	67 79 86
DP INT AUX P	DP 85D	DISPLAYPORT	67 83 86
DP INT AUX N	DP 85D	DISPLAYPORT	67 83 86
DP INT IG AUX P	DP 85D	DISPLAYPORT	79 82
DP INT IG AUX N	DP 85D	DISPLAYPORT	79 82
DP INT IG ML P<3..0>	DP 85D	DISPLAYPORT	79 82
DP INT IG ML N<3..0>	DP 85D	DISPLAYPORT	79 82
DP INT EG AUX P	DP 85D	DISPLAYPORT	74 79
DP INT EG AUX N	DP 85D	DISPLAYPORT	74 79
DP INT EG ML P<3..0>	DP 85D	DISPLAYPORT	74 79
DP INT EG ML N<3..0>	DP 85D	DISPLAYPORT	74 79
DP TBTSNK0 EG AUXCH P	DP 85D	DISPLAYPORT	74 80
DP TBTSNK0 EG AUXCH N	DP 85D	DISPLAYPORT	74 80
DP TBTSNK1 EG AUXCH P	DP 85D	DISPLAYPORT	74 80
DP TBTSNK1 EG AUXCH N	DP 85D	DISPLAYPORT	74 80
DP TBTSNK0 AUXCH P	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 AUXCH N	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 AUXCH C P	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 AUXCH C N	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 AUXCH P	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 AUXCH N	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 AUXCH C P	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 AUXCH C N	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 ML P<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 ML N<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 ML C P<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK0 ML C N<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 ML P<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 ML N<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 ML C P<3..0>	DP 85D	DISPLAYPORT	28 86
DP TBTSNK1 ML C N<3..0>	DP 85D	DISPLAYPORT	28 86

## Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
□	GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALIN 74 75
□	GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALOUT 74 75
□	GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT_R 74 75
□	GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_SSIN 74
□		1T01_DIEFFAIR		PEX_TSTCLK_O_P 68
□		1T01_DIEFFAIR		PEX_TSTCLK_O_N 68
□	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_P<2..0> 74 78
□	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_N<2..0> 74 78
□	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_P 74 78
□	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_N 74 78

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GPU (Kepler) Constraints			
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